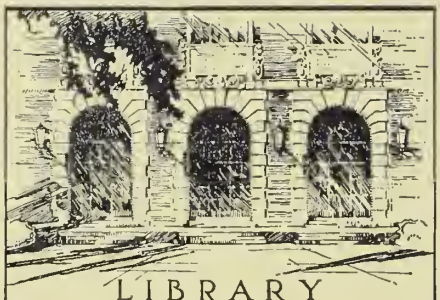

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THE VISTA SYSTEM FOR COMPRESSION OF TELEVISION SIGNAL BANDWIDTHS

by

DAVID CHARLES ROLLENHAGEN

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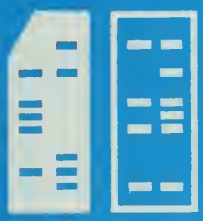

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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by

DAVID CHARLES ROLLENHAGEN

October, 1969

Department of Computer Science
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Urbana, Illinois 61801

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THE VISTA SYSTEM
FOR COMPRESSION OF TELEVISION SIGNAL BANDWIDTHS

David Charles Rollenhagen, Ph.D.
Department of Electrical Engineering
University of Illinois, 1969

The VISTA (Variable Interlace System for Television Applications) System compresses the bandwidth of television video signals in accordance with the amount of information change between successive television frames. The system automatically determines the information change and selects one out of sixty-four possible scanning speeds commensurate with this change. If the television information is constant, a large compression is possible, whereas a sudden change requires the full bandwidth of four MHz for a faithful reproduction of the television image. The system thus realizes the most efficient use of the television bandwidth.

Flicker and line drift effects at reduced scan rates are overcome by means of a variable persistence display device and by interlacing the fields in a programmable sequence. These techniques enable high quality reproductions of printed matter at bandwidths of up to eight-to-one.

A variable scan rate television camera is described and the signal current output of the vidicon as a function of scan rate is analyzed in detail. Also described in detail are the variable rate horizontal ramp generator and the automatic information change detector.

ACKNOWLEDGEMENT

The author is greatly indebted to Professor W. J. Poppelbaum, Principal Investigator of the Hardware Research Group and co-inventor of the VISTA system. His good counsel and friendship have led to a most enjoyable and rewarding four years at the University of Illinois. Few men undertake the combined roles of researcher and educator with more dedication.

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1. INTRODUCTION

The desirability of compressing the bandwidths of television video signals certainly requires no justification in this day and age where the over-crowded frequency spectrum is forever expanding to accommodate new bands. In fact, bandwidth compression has been the object of rather intensive study for some forty years. Evidently, it was clear at the outset that sufficient redundancy existed in television video signals to warrant such study. To date, however, there exists a wide gap between the recognition and actual quantitative measure of redundancy, and the practical means for utilizing this redundancy to achieve some economy of bandwidth. With the advent of information theory and in particular Shannon's work, means are now available for the measurement of redundancy and the theoretical determination of an upper bound to the possible bandwidth compression of television signals. Work in this area has now progressed to the extent that further advantage may be taken of the psycho-physical characteristics of vision beyond simply minimizing flicker. That is, redundancy exists due to man's inability to concentrate fully on the spatial, contrast, and motion characteristics of a television picture simultaneously.[1] Hence the recent interest in the statistical nature of typical television pictures.

Again, the fact remains that in spite of the theoretical advances with regard to redundancy and the possible bandwidth compression associated therewith, the practical realization of such bandwidth compression has lagged behind; not because of insufficient interest or talent in this area, but because of certain apparently insurmountable technical obstacles.

Nearly every system conceived thus far for the purpose of reducing television bandwidths realizes one or more of three basic types of redundancies: redundancy from element to element along a horizontal line, redundancy between horizontal lines, and redundancy from frame to frame.[2] The first two deal with picture areas, and the latter deals with picture motion between frames. It has been shown that a high degree of correlation exists in typical pictures for a run length of up to 50 elements per line, for 40 lines, and for 30 frames.[3] At first glance these figures could, theoretically, result in a tremendous economy of bandwidth. Only the most complex, and hence prohibitively costly, scheme could realize all three types of redundancy in an on-line fashion. To the extent of the author's knowledge, any workable scheme conceived thus far has dealt with, at most, only one of the three types of redundancy. The type most amenable to practical application is element-to-element redundancy along horizontal lines, though it has been suggested that the scheme due to Cherry and Gouriet[4] could easily be extended to cover element-to-element redundancy in both the horizontal and vertical directions.[5,6] Frame to frame redundancy is, perhaps, the most difficult to treat because some intermediate storage facility is required at the receiving end of the television system.

The most successful type of system involves detection of brightness changes along horizontal lines. The only video information required is the position and extent of areas of constant brightness along horizontal lines. Of course this in itself does not realize any economy of bandwidth, since many brightness changes may be concentrated in a small area of the picture, and the required bandwidth in such cases may be the full bandwidth. The brightness information must be redistributed along the time scale to effect a constant average flow of information. The value of this information rate depends on the

statistical nature of the picture. The particular scheme referred to above has led to a three-to-one bandwidth compression consistent with reasonably good quality pictures. One inherent problem of nearly any element-to-element redundancy scheme is the enhancement of the noise level during detection of brightness changes. As Professor Cherry so correctly points out, statistical methods must be employed in detecting brightness changes to reduce the effect of additive noise. Simple element-to-element differentiation schemes, for example, are not practical in any real communication link.[7,8]

Thus far, it appears that a three-to-one compression is the upper limit commensurate with a faithful reproduction of typical television broadcasts. Considering the inherent complexity of any practical system, it is questionable as to whether a three-to-one compression is economically worthwhile. Even more discouraging is the fact that such systems have realized little, if any, improvement over a simple high cut-off filter.[9] The picture may not be so bleak, however, and surely the discouraging practical aspects do not call for a termination of bandwidth compression studies. Television is finding greater and greater usage in areas which lend themselves to bandwidth compression schemes far better than does commercial television. Reproduction of printed matter, drawings, picture phone applications are good examples, to name a few. Many ham radio operators will testify to the usefulness of bandwith compression schemes.

A completely different class of bandwidth compression schemes aims not at a digital dissection of television pictures, but rather at a modification of the basic scanning process with no alteration of the resulting video signal. The pseudo-random scan,[10] the dot interlace scheme,[11] the four-to-one interlace scan[12] are systems which fall into this class. For systems of this class it is

no longer meaningful to speak in terms of redundancies, since the processes involved here are more adequately expressed in terms of the frequency domain rather than in terms of the time domain. Generally speaking, systems in this class realize a bandwidth reduction directly, usually through reduction and modification of the scanning velocity. Of course, these schemes, too, are not without their drawbacks. Two inherent problems are the inability to transmit picture motion without blur or jumpiness and the flicker problem associated with reduced scanning speeds.

The system described herein falls into the "frequency class" rather than the "time domain class" of systems. The objective of this project is to transmit the full signal bandwidth only when severe picture motion warrants its use. At other times the bandwidth is compressed, the exact amount of compression (and hence the choice of scan rates), depending on the severity of the picture motion. Should the entire picture change between successive television frames, the full (4 MHz) bandwidth is called for to reproduce this change without blur. Should only a small segment of the total picture area change between successive frames, the bandwidth may be reduced significantly without picture degradation. The bandwidth is compressed by reducing the scanning velocity in the television camera and receiver simultaneously. At reduced rates, the flicker problem is eliminated through the unique application of a variable persistence display device. In addition, the television fields are interlaced to help eliminate the downward drift of horizontal lines. The number of fields per frame depends on the scan rate, and hence the bandwidth. The exact interlace sequence is programmable to ascertain that sequence which optimizes the picture quality.

A question of economics presents itself in that the system must be capable of the full television bandwidth in the event of a complete picture change between successive television frames. This system in itself represents no economic gain, although its application in a larger system could realize a substantial gain. An observation of nearly any commercial television broadcast leads one immediately to the conclusion that very seldom is their sufficient motion, or enough complete picture changes to warrant the use of the full bandwidth. Possibly, many television signals could be monitored and statistically sampled for their respective bandwidth requirements. Each could then be shunted to an appropriate channel having the required bandwidth, and no more. It is not difficult to imagine many such schemes, but an elaboration beyond the immediate design and construction of the VISTA system is outside the scope of this project. Perhaps the most important motivating goal is to determine to what extent the bandwidth of the commercial television signal can reasonably be compressed using the reduced scan rate method and employing the variable persistence and programmable interlace features. A significant outsome of the project will be that particular interlace sequence most acceptable to the viewer. In addition, the project provides a valuable insight into technical problems associated with generating variable-rate waveforms and designing a camera operable at any one of many different scan rates.

2. VISTA SYSTEM OPERATION

A central problem in the design of the VISTA system was to derive a signal representing a measure of the amount of information change between successive television frames, hereafter referred to as the delta density signal, and to generate deflection voltages based on this measure. The deflection signals are then applied simultaneously to the deflection inputs of the television camera and monitor constituting the closed circuit system. Additional complexities centered around the primary objective of this study, namely the optimization of the television picture quality at reduced bandwidths by virtue of the persistence control and the programmable raster shift sequence.

Sixty-four different scanning speeds are provided, the fastest corresponding to the conventional rate, and the slower speeds derived by dividing the fastest rate by the integers, 1, 2, . . ., 64. If the delta density signal indicates a complete change of information, the fastest rate is selected. Otherwise one of the slower rates is selected depending on the relative magnitude of the delta density signal.

Figure 2.1 presents a simplified block diagram of the VISTA system. The television camera is used for two different purposes. It provides a signal to enable the delta density detector to measure the information change between frames. In addition, it is used as a slow scan camera during the bandwidth compression process. Thus the system alternates between a fast scan mode during which the information change is sampled, and a slow scan mode during which the bandwidth is compressed on the basis of the sample. This alternation is not observed by the viewer since the same picture is displayed regardless of the rate at which it is scanned. One of the many unknowns of the system was the number of frames required for the vidicon tube in the camera to settle

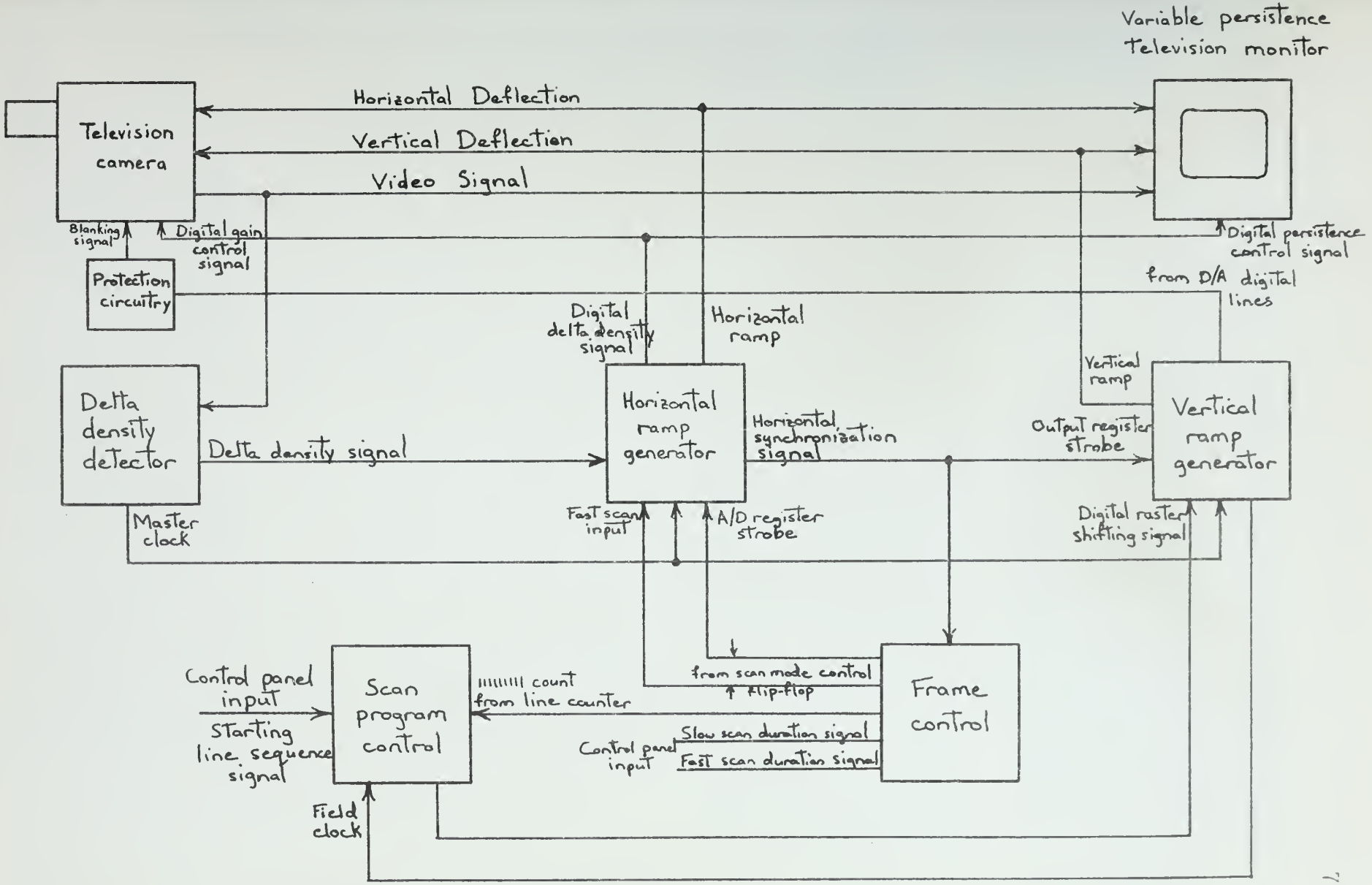


Figure 2.1 Simplified Block Diagram of the VISTA System

down to steady state operation at any one scan rate. Obviously, a continually changing scan rate would be intolerable. The minimum number of complete frames required for steady state operation is ascertained and preselected by the operator for each mode independently. The system may be programmed to reside in each mode for a total of from one to sixty-four complete frames. This is the origin of the scan duration signals leading to the frame control block in Figure 2.1.

The variable scan rate nature of the system dictated a rather elaborate scheme for realizing the programmable interlace feature of the system. In general, one complete frame in which all 512 lines are scanned is divided into x fields, x being the scan rate reduction factor. (For a three-to-one compression ratio, for example, the scan rate is one third of the conventional rate. Here x is three.) In any one of the x fields, every xth line is scanned, the total being 512/x lines scanned per field. All x frames are interlaced in a manner determined by the system operator. The starting line sequence signal shown leading to the scan program control block in Figure 2.1 causes each successive raster to interlace in such a manner that the bar drift effect is minimized at reduced scan rates. The starting line input on the control panel is a program in the truest sense of the word, since the pattern must be valid for any scan rate reduction factor x. Two typically useful starting line sequences are 1, n, 2, n-1, 3, n-2, . . ., n/2, n/2 + 1, and n, n-1, n-2, n-3, . . ., 2, 1.

The vertical deflection signal is a stair-step ramp, each step corresponding to a horizontal line. Due to the interlacing pattern described above, the vertical ramp period is constant, but the number and height of the stair-steps vary with the scan rate. The raster shift is implemented very simply by shifting the dc level of each ramp. This results from the application

of the digital raster shifting signal to the vertical ramp generator shown in Figure 2.1.

In addition to the programmable interlaced scan, the standard line sequential pattern may be selected by the operator to function at any one of the sixty-four scan rates. A comparison between the variable interlace scheme and the line sequential system clearly indicates the degree of improvement over the latter.

A unique application of the Hewlett-Packard Model 181A variable persistence oscilloscope was its use as a variable persistence television monitor. The device is, essentially, a storage oscilloscope with a facility for varying the erasure rate of the stored information. A digital form of the delta density signal is available for controlling the persistence and for controlling the gain of the television camera for different scan rates as shown in Figure 2.1.

3. SUBSYSTEMS

3.1 Delta Density Detector

The central component of the delta density detector, as shown in the block diagram in Figure 3.1.1, is the video disc recorder. During each fast scan mode of operation the video signal originating in the camera is simultaneously stored and compared with the video signal which was recorded during the previous fast scan. This comparison of video signals eventually leads to a measure of the amount of information which changes between successive fast scans. The disc control shown in Figure 3.1.1 shunts the video signals between three of the four tracks on the recorder. The fourth track is not used, and a fifth track provides synchronization signals for the entire system. Details of the disc control appear in the Appendix.

The two signals to be compared arrive at the compare and hold circuit illustrated in Figure 3.1.2. The signals are of opposite polarity and pass through a normalization and buffer stage whereupon they are added at the operational amplifier. The resulting signal is rectified to provide a positive voltage in the event that the difference is negative. Thus the absolute value of the signal difference is realized. Diodes D_1 and D_4 are included in a unique arrangement to insure that the rectified current through R in the bridge is precisely equal to the difference current through R in the feedback loop. This being true, the voltage drop across D_1 exactly equals that across D_6 when the operational amplifier output is positive and D_2 and D_6 are forward biased; the voltage drop across D_4 exactly equals that across D_5 when the operational amplifier output is negative and D_3 and D_5 are forward biased. Moreover, the diodes are temperature compensated, each being a member of a six-diode array.

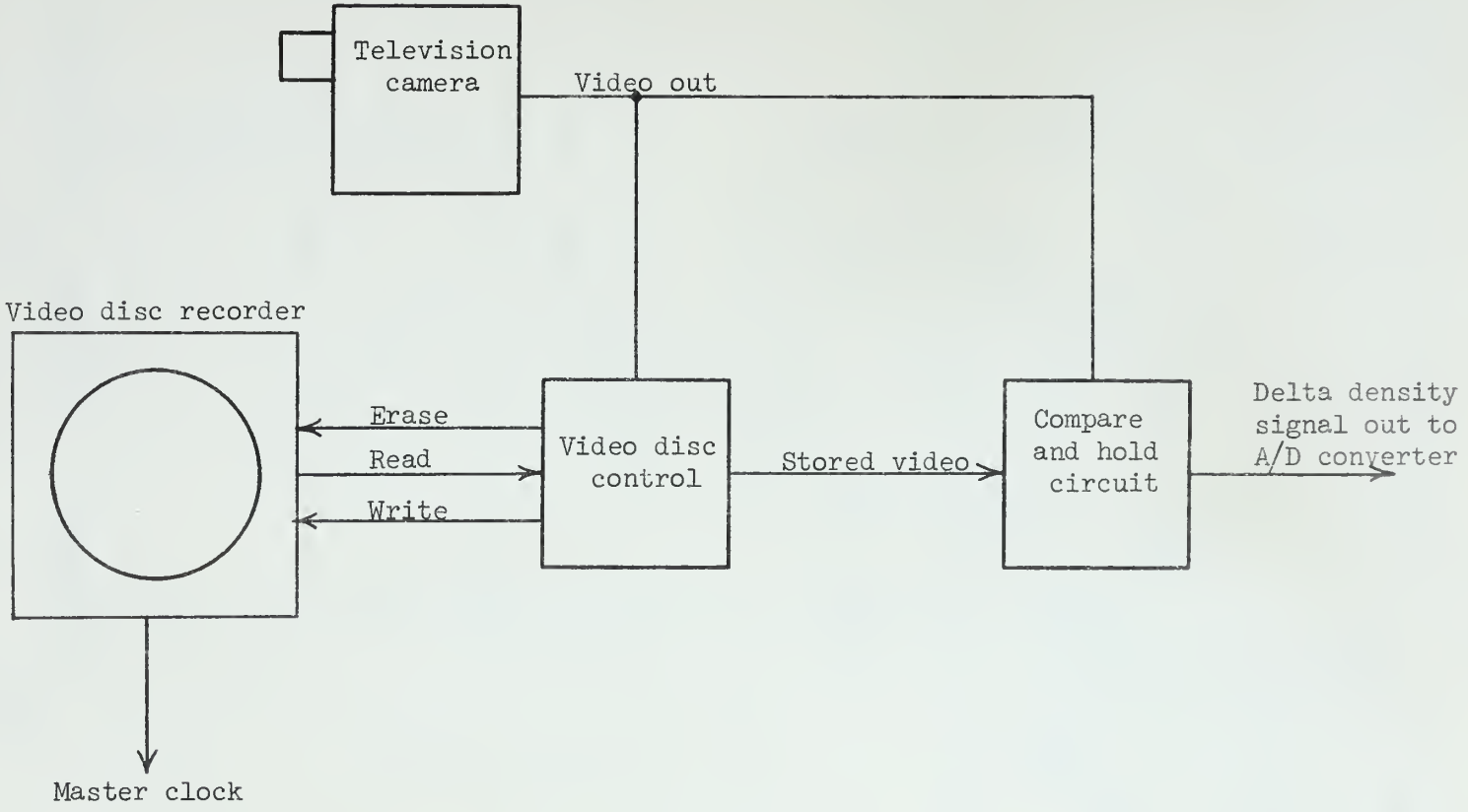


Figure 3.1.1 Block Diagram of the Delta Density Detector

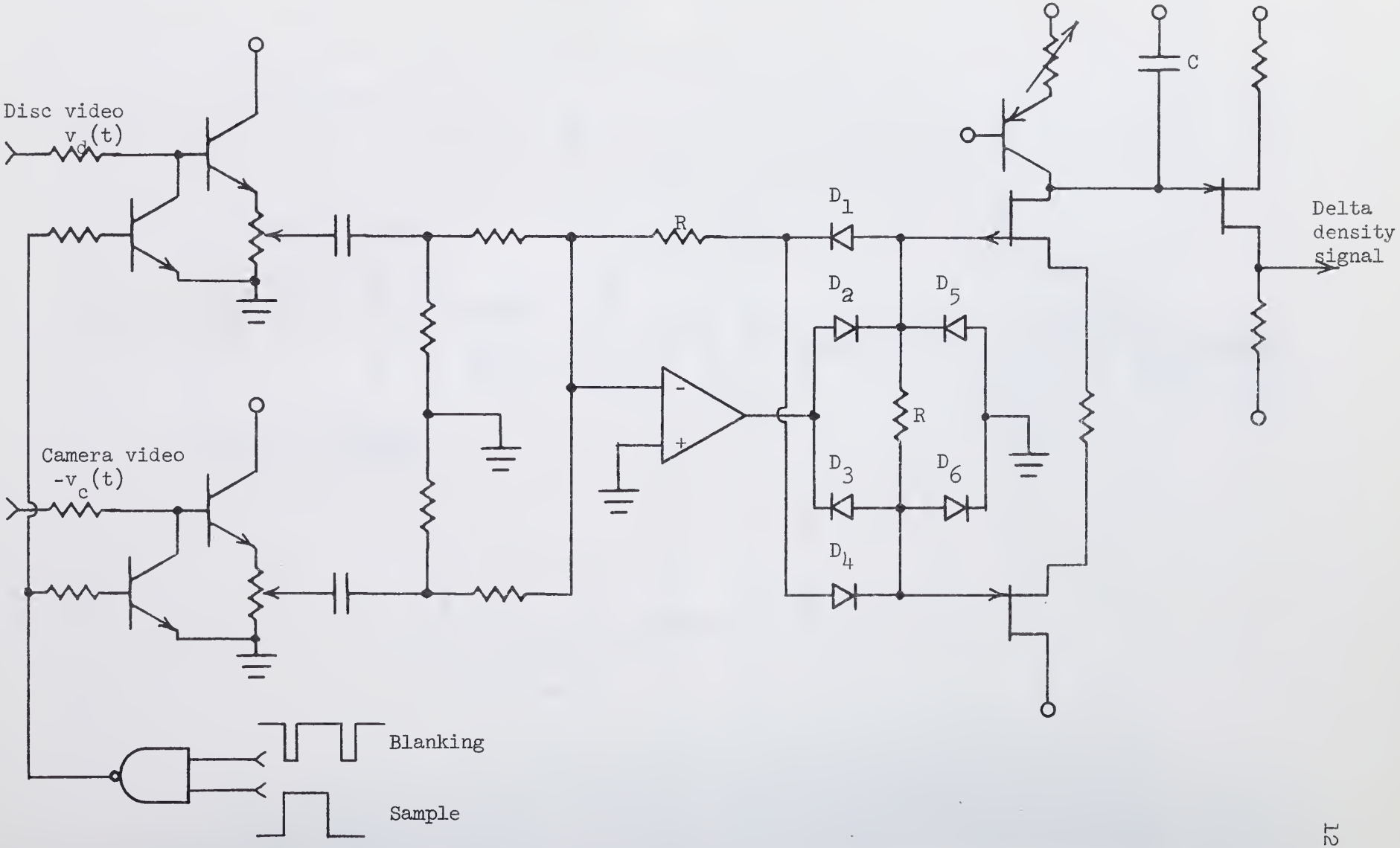


Figure 3.1.2 Compare and Hold Circuit

The magnitude of the difference voltage appearing across R of the bridge is detected and integrated by virtue of the field effect transistor arrangement which follows. The shifting nature of the voltage difference dictated the choice of this arrangement. In addition, the high impedence input to the complementary field effect pair prevents undesirable offset currents from appearing at the bridge. The bias current for this pair is supplied by the transistor current source. Any non-zero voltage across R results in a charging current through C. For small signal voltages across R, the resulting voltage across C will be

$$\int_0^T |v_d(t) - v_c(t)|dt$$

The video signals are attenuated at the input to the operational amplifier to insure that the linear range of the field effect transistors is not exceeded. The last field effect stage is a high impedence readout amplifier.

A gating voltage is applied at the input to the compare and hold circuit so that no comparison is made during the blanking period (since the blanking voltages may be unequal) or during the slow scan mode. The voltage across C, representing the delta density signal, will thus be stored during these intervals. The gating voltage cuts off the two input buffer transistors simultaneously, resulting in zero volts at the operational amplifier input when the digital output of the NAND gate is a logical "1".

3.2 Variable Rate Horizontal Ramp Generator

The waveform required of the variable rate horizontal ramp generator is a sawtooth of constant amplitude whose period is inversely proportional to the delta density signal, or inversely proportional to the rate at which the television information changes. The basic scheme involves a constant current source charging a capacitance. The only feasible method for realizing the variable rate nature of the waveform consistent with the required proportionality relationship was to switch binary weighted capacitors into the charging circuit. Seven digitally controlled transistor switches were applied to the circuit as shown in Figure 3.2.1. While these elements were sufficient to generate the specified slope, a rather different technique was employed for maintaining a constant amplitude and synchronizing the waveform to the master clock. The six-bit counter is reset at the conclusion of every horizontal period. The count is incremented every clock period until the count coincides with the digital number $\overline{N}$, at which time a horizontal synchronization pulse is generated which activates the retrace circuit shown in Figure 3.2.2. The capacitance is then linearly discharged, and the resulting waveform is the desired linear retrace ramp having negative slope. Upon reception of a horizontal synchronization pulse, the RS flip-flop is set which opens the capacitor discharge gate allowing a constant current to discharge the capacitance. The linear discharge proceeds until the ramp voltage reaches a minimum value established by V_{ref}. At this time the differential comparator furnishes a pulse to reset the RS flip-flop and close the discharge gate. The discharge current source is then removed from the circuit, and the linear charge process recommences.

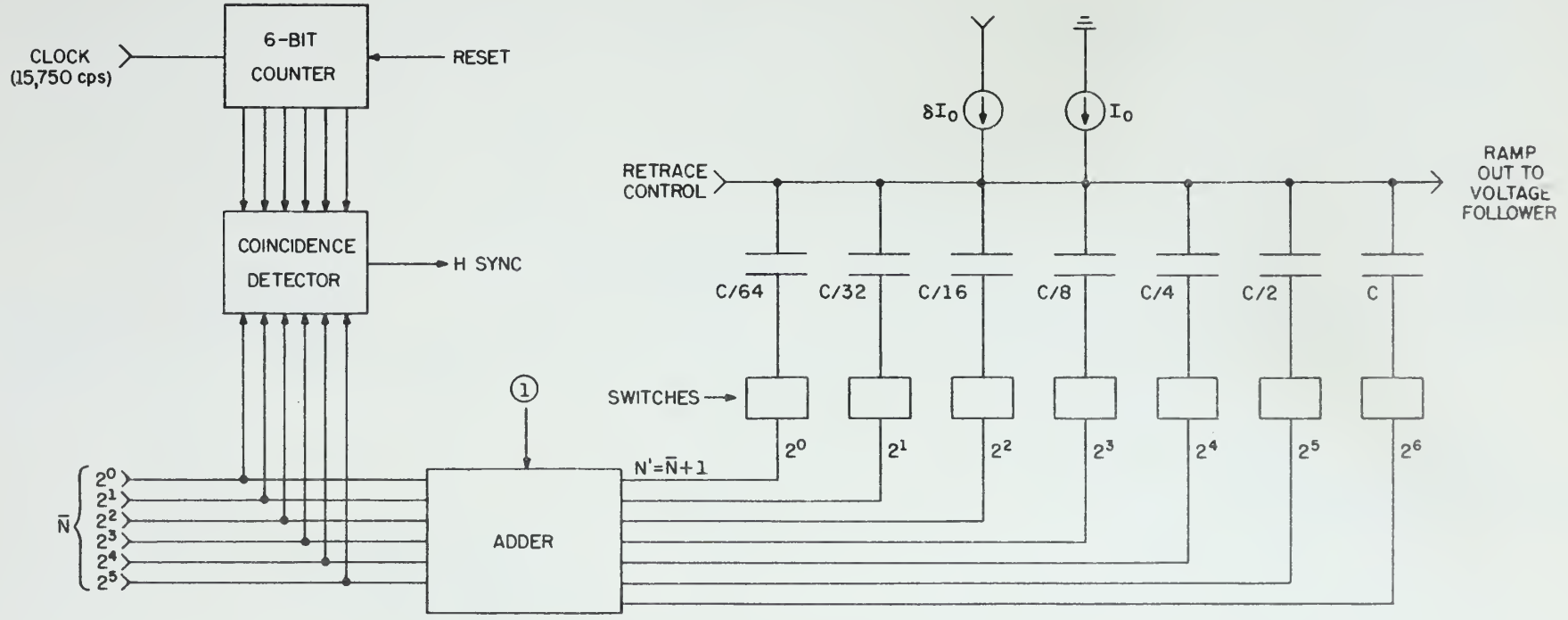


Figure 3.2.1 Variable Rate Horizontal Ramp Generator

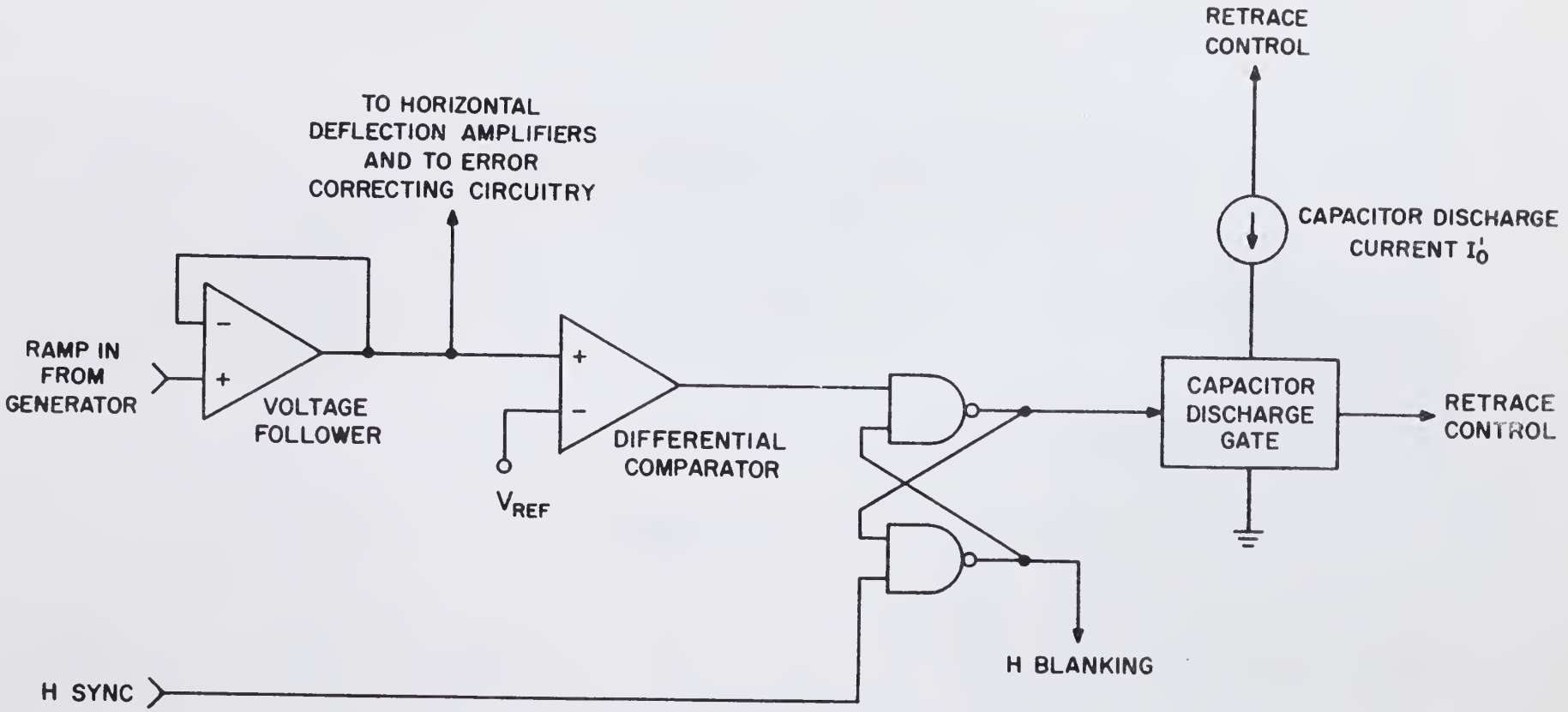


Figure 3.2.2 Retrace Circuit

This unique scheme for generating the horizontal ramp enjoys two distinct advantages over any other arrangement. First, the retrace period is always a fixed proportion of the entire ramp period (namely 15.8 percent) regardless of the scan rate. This follows from the fact that regardless of the magnitude of the capacitance, all capacitance values are charged and discharged by the same two constant current sources. Second, for sudden disruptions in the system which may cause a faulty count or any other spurious non-periodic error, the circuit is self-correcting. This is a direct result of the geometry of the waveform which is illustrated in Figure 3.2.3. Here the period is designated T, the ramp slope a, the retrace slope fa, and the voltage amplitude V. Assume a sudden displacement at the beginning of the ramp (so chosen for the sake of convenience) of magnitude δT. When retrace is initiated by the coincidence circuit, a voltage error $\delta V_1 = a\delta T$ results. During the second period the error in the ramp period is $\delta T_2 = -\frac{\delta V_1}{fa}$ which leads to a voltage error $\delta V_2 = -\frac{a\delta T}{f}$. Continuing in a similar manner,

$$\delta V_3 = +\frac{a\delta_2 T}{f}$$

$$\vdots$$

$$\delta V_n = (-1)^{2n+1}\frac{a\delta T}{f^{n-1}} .$$

Thus after n periods, the voltage error has been reduced by a factor of f^{n-1}. Since f = 5.35, the initial voltage error is reduced by a factor of 28.6 after three complete periods.

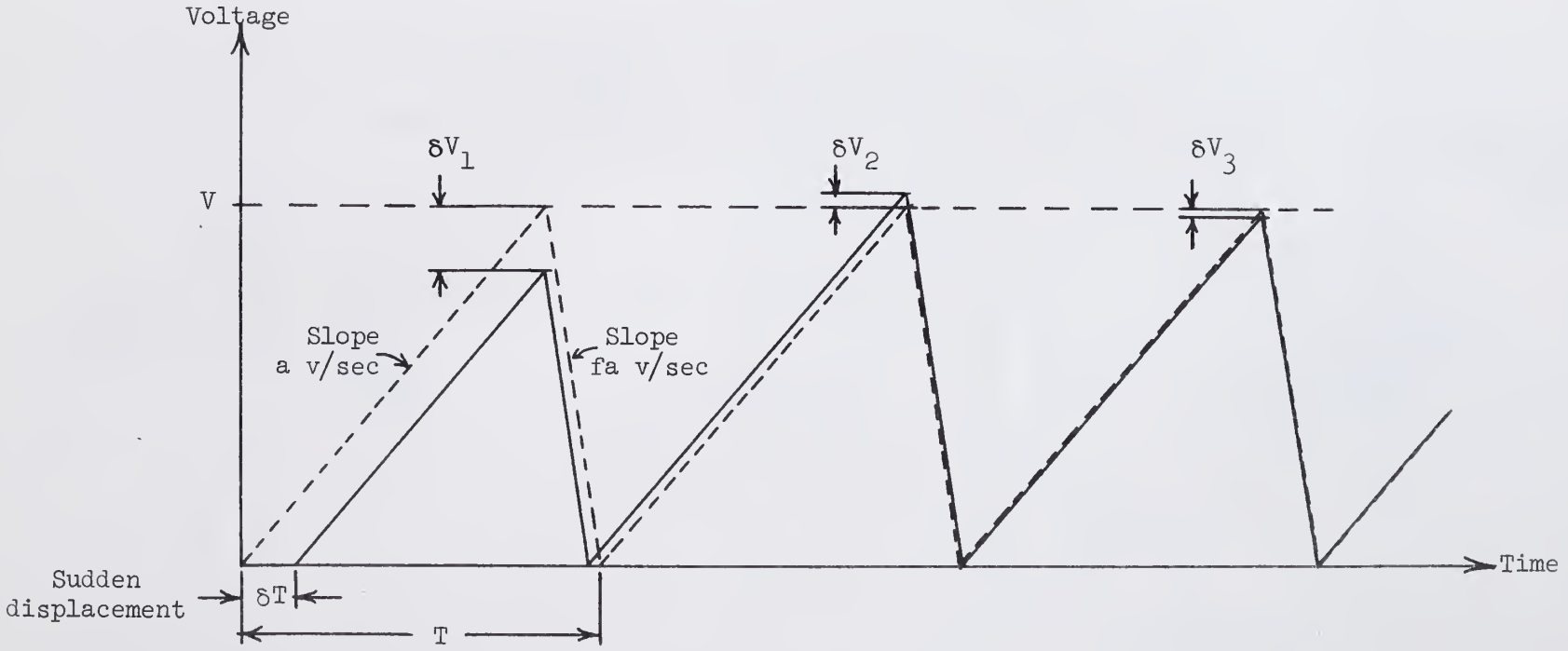


Figure 3.2.3 Waveform Illustrating Self-Correcting Nature of Horizontal Ramp

A second type of error is a periodic error due, for example, to an incorrect capacitance value. The result is an error in the voltage amplitude, the error being constant for any one scan rate, but different for different scan rates. Such an error was, in fact, detected although the resulting horizontal gain variation of the picture for different scan rates was not considered objectionable. A rather elaborate scheme for correcting such an error was devised, however, in the event that it proved necessary. This scheme and some theoretical results are presented in the Appendix. Had it actually been employed, this would have been the source of the error correcting current δI_0 shown in Figure 3.2.1.

Finally, a word concerning the origin of the digital numbers which control the scan rate. Figure 3.2.4 shows the logic elements located between the A/D converter and the horizontal ramp generator. $N = n_5 2^5 + n_4 2^4 + n_3 2^3 + n_2 2^2 + n_1 2^1 + n_0 2^0$ is the binary number which emerges from the A/D converter. Having proceded through all the intervening stages, it arrives at the capacitor switches transformed to the number $N' = n'_6 2^6 + n'_5 2^5 + n'_4 2^4 + n'_3 2^3 + n'_2 2^2 + n'_1 2^1 + n'_0 2^0$ which equals $\bar{n}_5 2^5 + \bar{n}_4 2^4 + \bar{n}_3 2^3 + \bar{n}_2 2^2 + \bar{n}_1 2^1 + (\bar{n}_0 + 1)2^0$. Both numbers N and N' posses 64 possible states, but their respective decimal equivalents are zero to 63 and one to 64. An addition of the binary digit 1×2^0 to the number N, following an inversion, results in a signal N' which may be used to control the binary weighted capacitors directly. Otherwise the zero state of $\bar{N}$, while being a perfectly admissible binary number, would not be a useful state in the switching of a capacitor. The result is, of course, a seven bit number. If τ is the ramp period, τ may be simply expressed in terms of the circuit parameters and the number N' as

$$\tau = \frac{VC}{64(I_0 + \delta I_0)}[64n'_6 + 32n'_5 + 16n'_4 + 8n'_3 + 4n'_2 + 2n'_1 + n'_0]$$

$$= \tau_{min}[64n'_6 + 32n'_5 + 16n'_4 + 8n'_3 + 4n'_2 + 2n'_1 + n'_0]$$

Table 3.2.1 lists several exemplary binary numbers N, the respective conversions N', and the corresponding ramp period τ.

The NAND gates immediately following the buffer register in Figure 3.2.4 were originally intended simply as inverters. However, the gates were found ideally suited as an input for switching the system between the slow and fast scan modes. With the fast scan gate at a logical "0", the outputs of the NAND elements must be logical "1"'s regardless of the number N. The resulting binary number is $N' = 0 \cdot 2^6 + 0 \cdot 2^5 + 0 \cdot 2^4 + 0 \cdot 2^3 + 0 \cdot 2^2 + 0 \cdot 2^1 + 1 \cdot 2^1$ corresponding to $\tau = \tau_{min}$, the desired horizontal ramp period in the fast scan mode. On the other hand, with the fast scan gate at a logical "1", the NAND elements behave as simple inverters in the conversion from N to N' during the slow scan mode.

3.3 Frame Control

The number of frames scanned in each of the slow and fast scan modes is initiated by the operator at the control panel and implemented by the frame control subsystem. The scan mode control flip-flop, one of the most important single elements in the system, is contained within this subsystem. Figure 3.3.1 illustrates the mechanism by which the scan mode control flip-flop switches the entire system between the slow and fast scan modes at the conclusion of the preselected number of frames. The line counter and the 111111111 count detector determine a complete frame of 512 scan lines. Each pulse corresponding

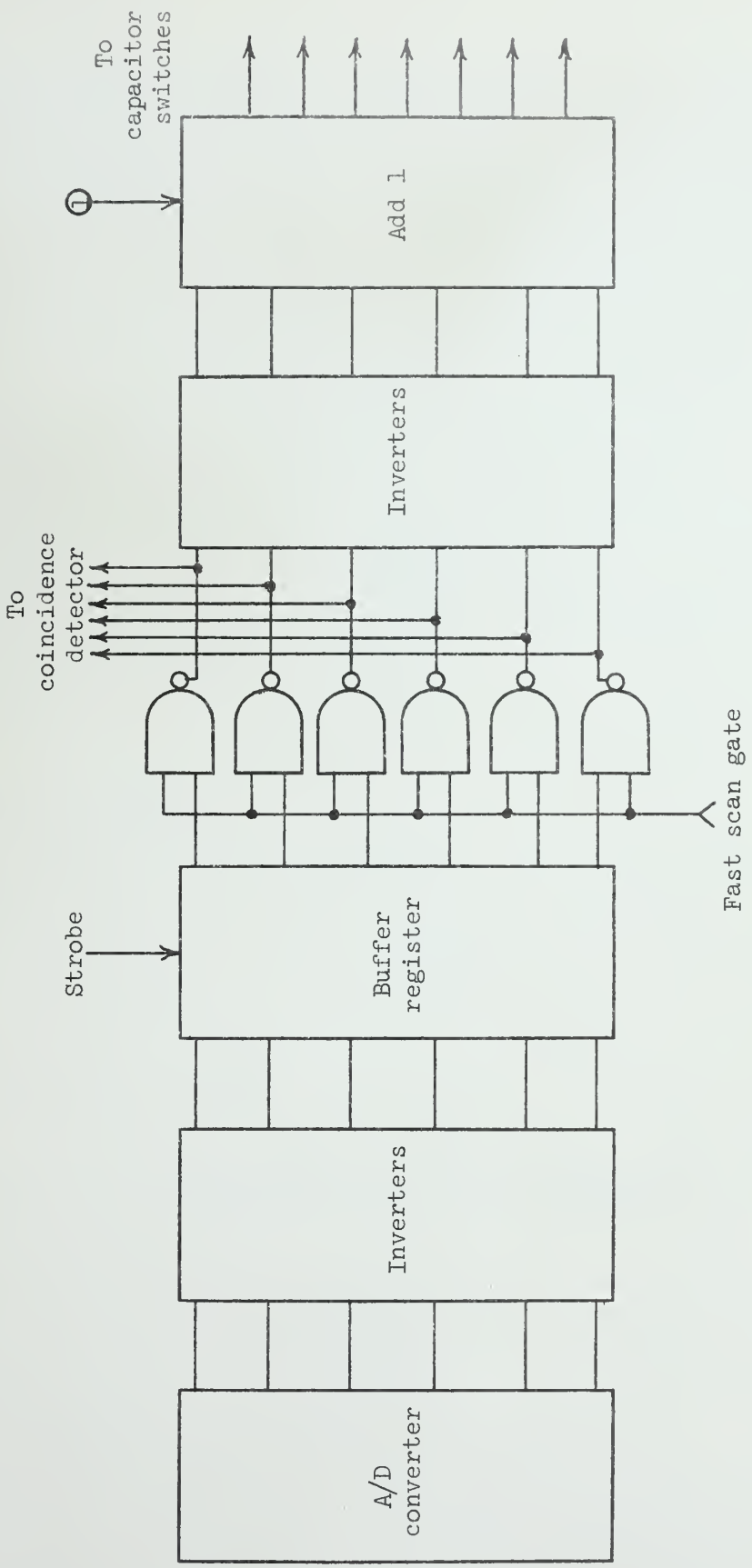


Figure 3.2.4 Derivation of Binary Numbers for Horizontal Ramp Generator

N	N'	τ
000000	1000000	64 τ_{min}
000001	111111	63 τ_{min}
000010	111110	62 τ_{min}
.	.	.
.	.	.
.	.	.
111110	000010	2 τ_{min}
111111	000001	τ_{min}

Table 3.2.1 Exemplary Binary Numbers Used in the Derivation of the Horizontal Ramp

to the completion of one frame then increments the 6-bit frame counter. When the output of the frame counter coincides with the scan duration signal set by the operator for each mode, a coincidence pulse occurs indicating that the prescribed number of frames has been scanned. At this time the scan mode control flip-flop changes states for the beginning of a new frame count in the alternate mode. A Q output of "1" corresponds to the fast scan mode during which time the fast scan gate is actuated and the fast scan duration signal enters the coincidence detector circuit. When the Q output becomes a logical "0" the slow scan mode begins at which time the A/D register containing the digital delta density signal is strobed, and the slow scan duration signal enters the coincidence detector circuit.

3.4 Vertical Ramp Generator

Among other responsibilities demanded of the vertical ramp generator is that it shift each successive raster up or down in accordance with instructions received from the scan program control. The means for achieving this result is the 9-bit adder illustrated in Figure 3.4.1. A digital count corresponding to the specified starting line of each field is added to the output of the 9-bit counter.

The addition of the starting line count simply shifts each raster down by a specified number of lines at the beginning of each field. As this number changes, the level shift of the raster changes accordingly. The input register is strobed when the counter overflows and when the scan mode control flip-flop is in that state corresponding to the slow scan mode.

The 9-bit counter produces a stair-step voltage ramp at the output of the D/A converter. The length and height of the steps is determined by the periodicity of the horizontal synchronization pulse which strobes the output

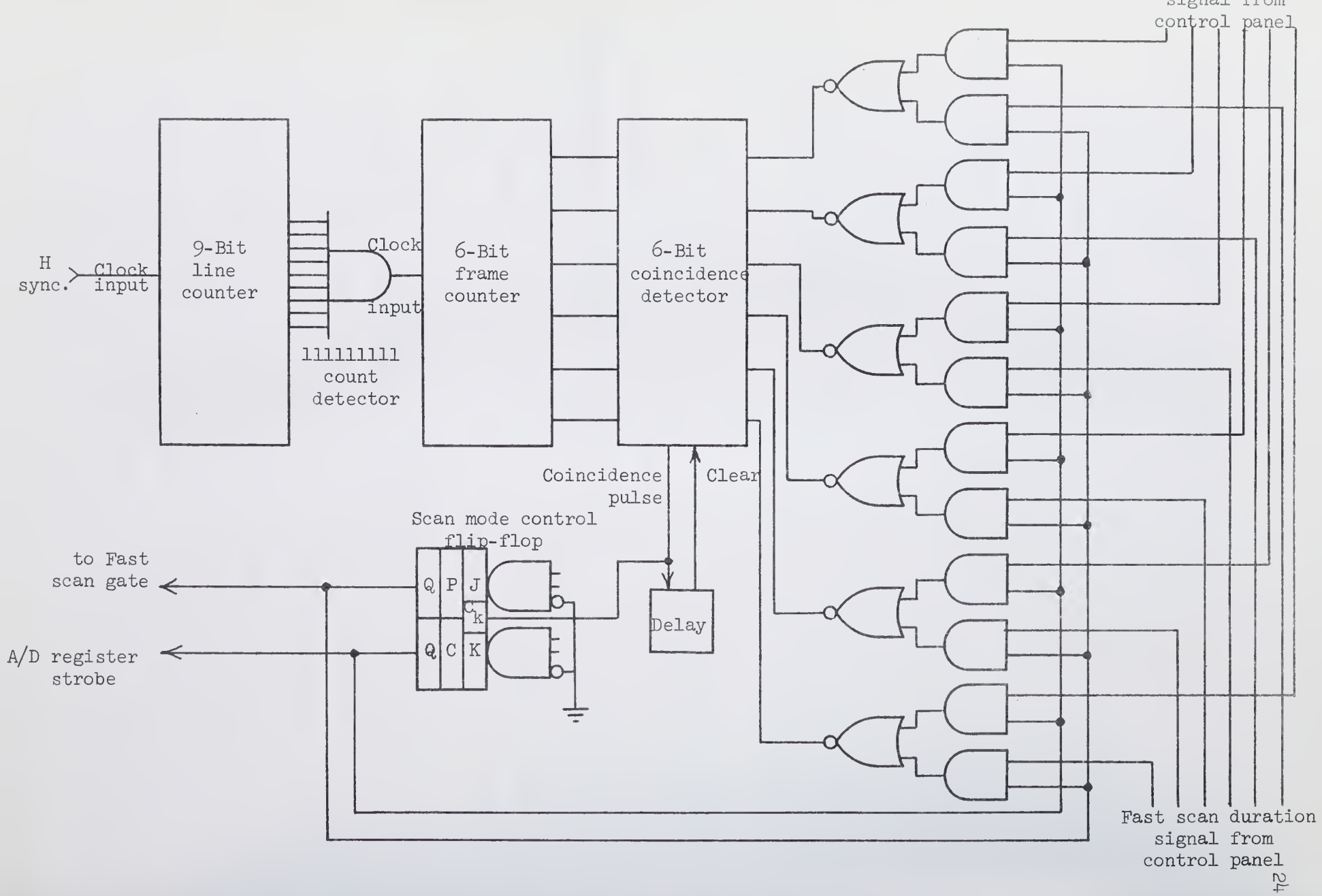


Figure 3.3.1 Block Diagram of Frame Control

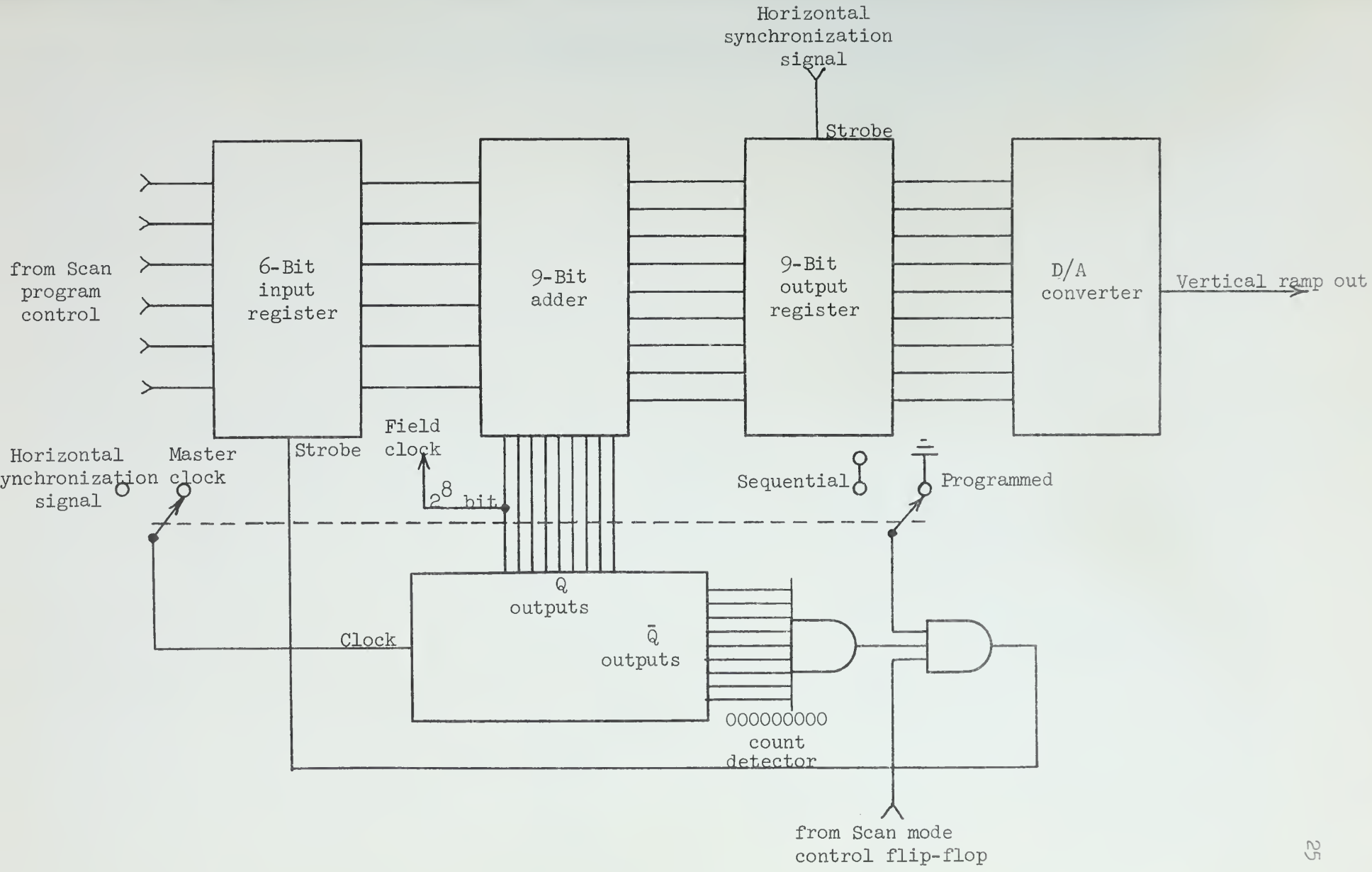


Figure 3.4.1 Vertical Ramp Generator

register at the end of each horizontal line. If the register is strobed every nth clock period, for example, corresponding to an n-to-one compression, the steps will be n times as long and n times as high as those for a one-to-one compression. The result is that every nth line is scanned. Except in the line sequential type scan, the ramp period remains fixed for all time. The counter overflows after 512 counts to begin a new vertical ramp period.

The standard line sequential pattern is easily implemented at any scan rate by locking out the input register strobe and counting horizontal synchronization pulses in place of master clock pulses as shown in Figure 3.4.1.

3.5 Scan Program Control

The sole purpose of the scan program control is to implement the interlace sequence programmed by the system operator. Basic to this scheme is the use of two 6-bit up-down counters in the derivation of the required digital number at the beginning of each field. Either one or the other or an alternate use of both counters may be employed in the scan program. The essential elements of the scan program control are shown in Figure 3.5.1. The AND-OR-INVERT gates shunt the outputs of the appropriate counter to the input register of the vertical ramp generator. The state of the jk flip-flop determines which counter is being employed. In the event of an alternate use of both counters, the flip-flop is clocked once each field, and the counters are alternately switched to the common output leading to the vertical ramp generator. In this manner, a starting line sequence such as the following may be realized: 1, n, 2, n-1, 3, n-2, . . ., n/2, n/2+1. In this particular example, counter number 1 is set to count up from line number 1, counter number 2 is set to count down from line number n. Counter 1 is switched into the circuit during the first field, counter 2 is switched in during the second field, then back to counter 1

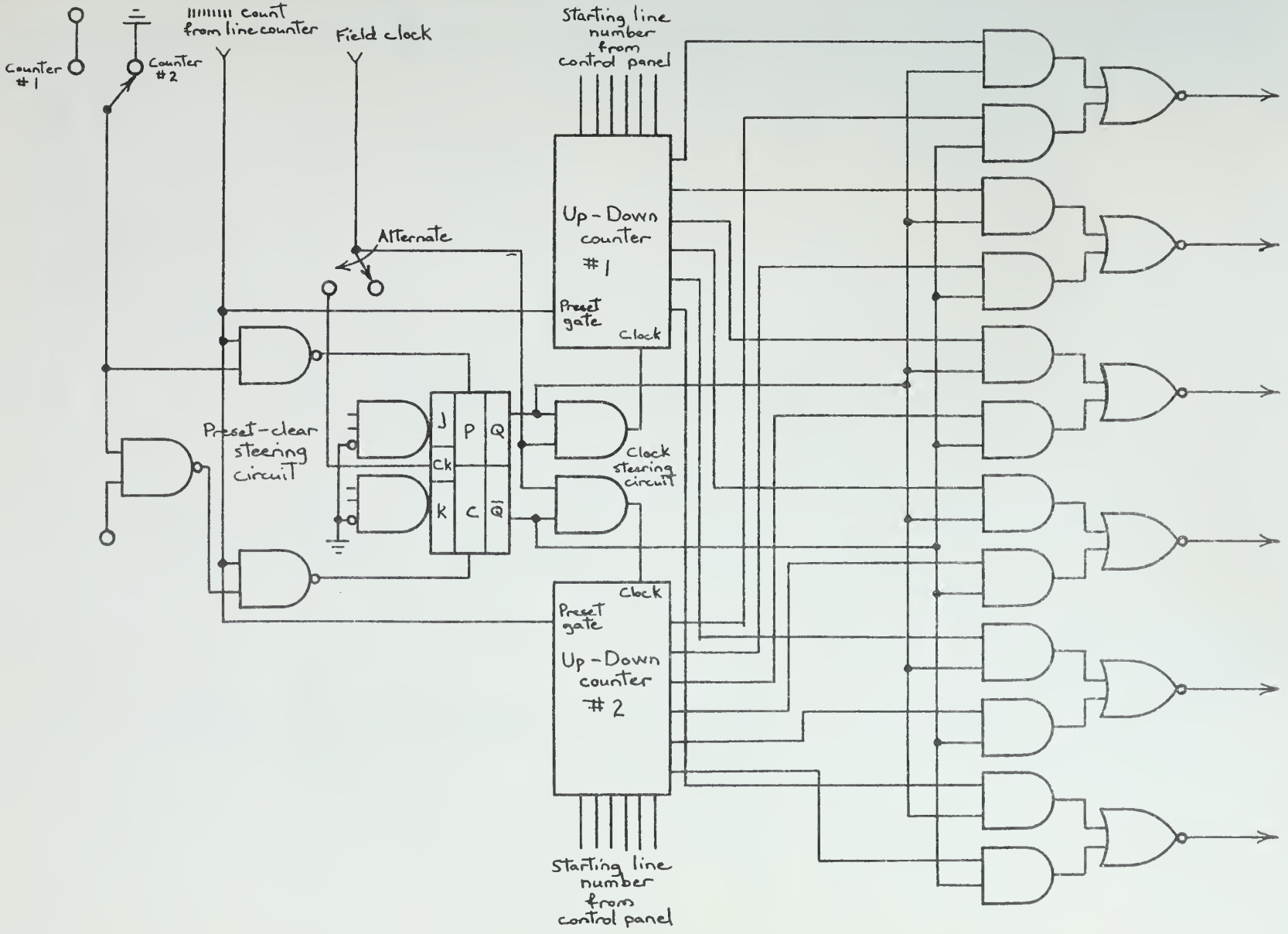


Figure 3.5.1 Scan Program Control

and so on. Each counter is clocked once every other field in this alternate program. If only one counter is used to implement a starting line sequence of 1, 2, 3, . . ., n, for example, the jk flip-flop remains in the state to which it was initially preset or cleared (corresponding to the use of counter 1 or counter 2, respectively) and the counter being used is clocked once every field.

The initial contents of each counter are set via the starting line switches on the control panel. The clock steering circuit shunts the field clock signal to the appropriate counter, depending upon the state of the jk flip-flop. During single counter operation the preset clear steering circuit sets the state of the flip-flop, thus selecting one of the two counters and steering the field clock accordingly.

3.6 Variable Scan Rate Television Camera

The variable scan rate television camera was designed and built to operate at any one of 64 possible scan rates, the maximum rate being that of the conventional television system; namely, 15,750 horizontal television lines per second. Slower rates were derived by dividing the maximum rate by the integers 2, 3, . . ., 64. The deflection waveforms and blanking signal corresponding to these different rates were supplied to the camera by the main frame. The camera itself consists of a power supply, four deflection amplifiers, a preamplifier, amplifier, gain control circuitry, protection circuitry, and the all-electrostatic vidicon tube. A block diagram of the camera system is shown in Figure 3.6.1.

The central problem encountered in the design of the camera was to maintain a constant signal level for all possible scanning rates. Without the use of a variable speed mechanical shutter, it was questionable as to whether or not the signal amplitude, extracted at the vidicon target, would remain

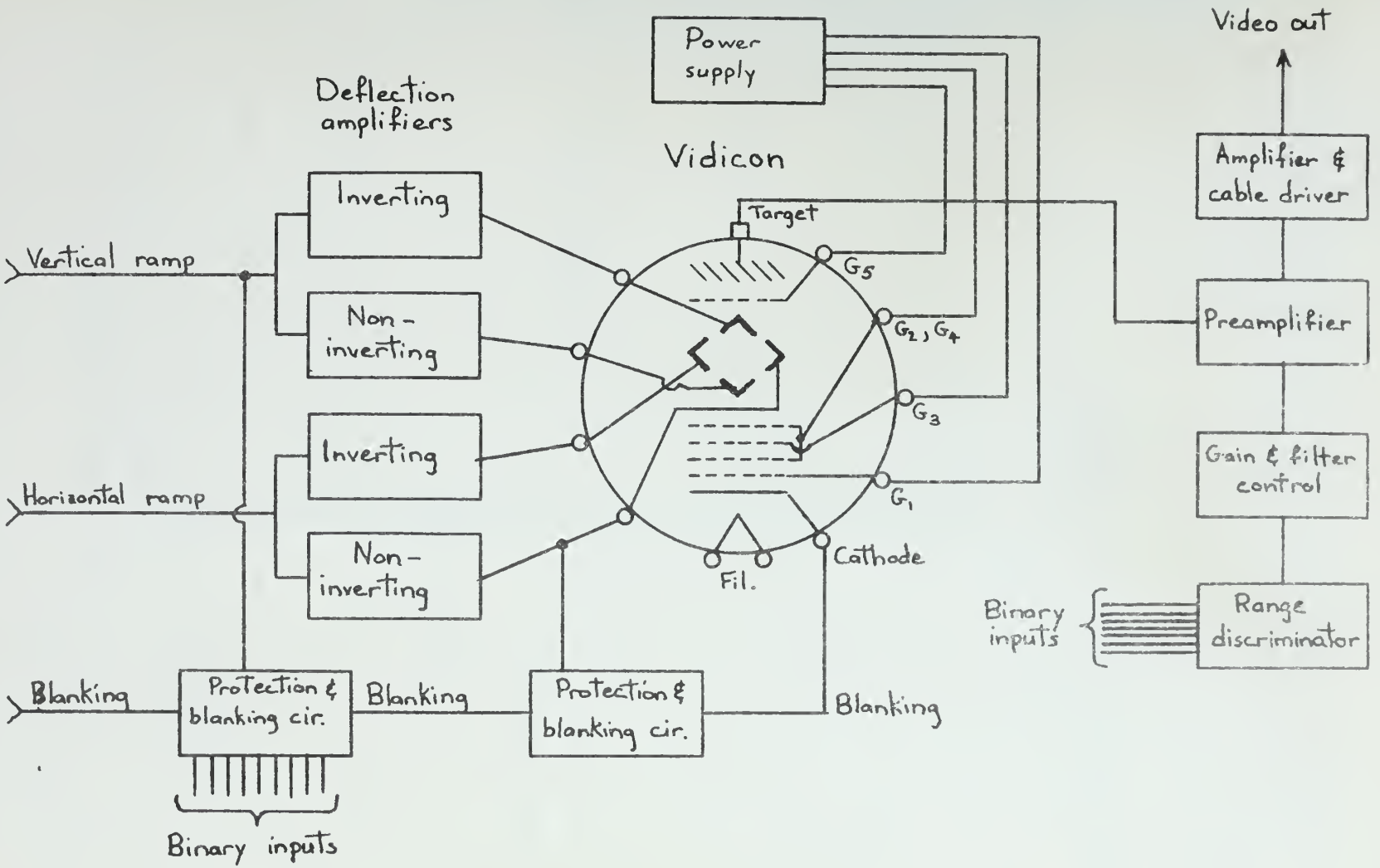


Figure 3.6.1 Block Diagram of Variable Scan Rate Camera

the same for the various scan rates. The following section is devoted to an analysis of this problem in terms of the dynamic characteristics of the vidicon tube.

3.6.1 Signal Level as a Function of Scan Rate

A brief review of the dynamic operation of the vidicon will establish the basis for the following analysis.

The vidicon target consists of a photoconductive deposition backed by a transparent conductive coating which is electrically connected to the target flange. This results in an effective capacitance from one side of the target surface to the other, with the photoconductor acting as a dielectric. Figure 3.6.1.1 shows the physical aspects of the target along with the external circuitry and the equivalent circuit of each small target element. Incident light focused on the target causes a certain leakage or conduction to occur through the photoconductive material at each small location, the exact amount depending on the intensity of the incident light at that location. The resistance R_L of each element, a function of the light intensity at that point, accounts for this leakage. The signal voltage, $v_S(t)$, is extracted across resistance R_S as the beam impinges on the target surface, recharging the capacitance C of each element that it strikes. The beam side of each element is charged down to cathode potential, or zero volts, while the conducting side is returned to the target voltage, V_T. Resistance R_D accounts for the so-called dark current which adds to the signal current, producing the signal voltage. The dark current is generally small compared to the signal current if the target is constantly illuminated.

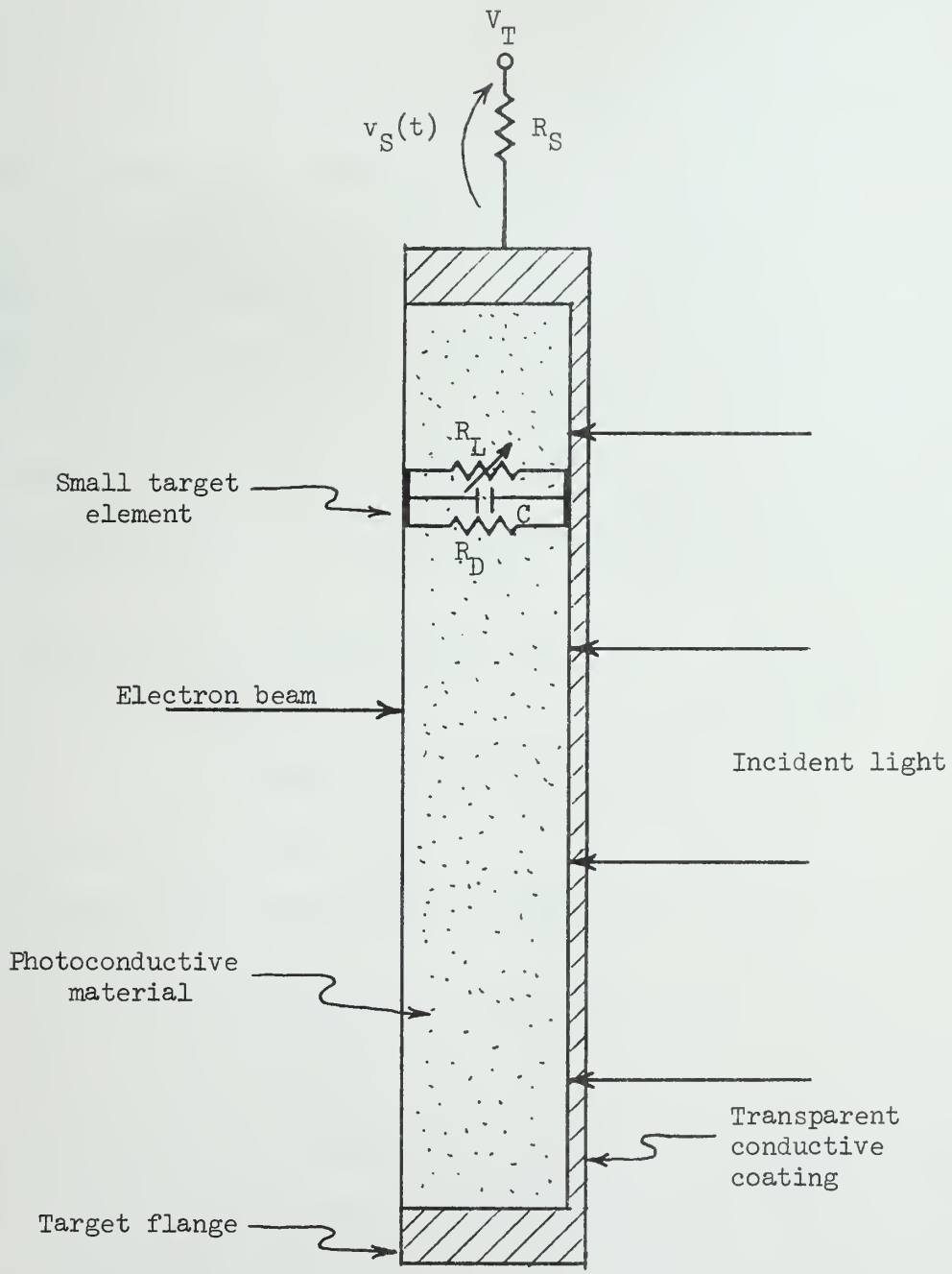


Figure 3.6.1.1 The Vidicon Target and Associated Circuitry

The target voltage, V_T, is typically 30 volts. The incident light causes the capacitance C of each element to be discharged from 30 volts in the manner of an exponential decay. At reduced scan rates, the incident light integrates over a longer period of time, resulting in a larger voltage decay. When the light is permitted to integrate in this manner, the frame rate must not be so low that the voltage across the target decays by more than several volts, otherwise the resulting electric fields will become sufficiently large to distort and defocus the electron beam. Since this decay may not exceed roughly 10 percent, the discharge occurs over a nearly linear portion of the exponential decay. The extent to which a linear approximation is valid is termed "linear storage". The salient implication here is that to a point, the voltage decay is nearly a linear function of frame time, assuming constant illumination.

The recharging process occurs as the beam strikes each element of the target surface. Charging occurs until the surface is brought down to cathode potential. If it can be shown that the voltage increment by which C is recharged each frame is a linear function of frame time, then this recharge will exactly compensate the linear discharge, regardless of the frame time or scan rate. It then follows that the signal level cannot be a function of scan rate, assuming constant illumination and linear storage. Evidently, this result is well known to those experienced in the field of television pickup tubes, although to the best of this author's knowledge, no detailed explanation has been set forth.[13,14] The following simple analysis will show, to a good approximation, that the increment by which C is recharged each frame is proportional to the frame time.

Figure 3.6.1.2 shows the complete circuit for any one element of the target. The current source and the diode represent the effect of the impinging electron beam. Assume that the function $i_0 f(\xi)$ represents the spatial current distribution of the spot in the ξ direction through the center of the spot. As a function of time, therefore, the current impinging on each element may be represented by the waveform shown in Figure 3.6.1.3. (This figure neglects distortion of the beam as a function of velocity in the direction of motion.) Here again x is the scan rate factor. At time $t = nxT + xt_0$, a frame time of xT seconds, diode D becomes forward biased, and the video signal $v_S(nxT + xt_0) = i(nxT + xt_0)R_S$ is maximum. R_D and R_L are very large, and may be neglected during the charging process. The signal voltage developed across R_S is generally small compared to the voltage developed across C, in which case $v_S(t)$ may also be neglected. Under these conditions, the voltage increment by which C is charged during each charging interval is

$$v_C(nxT + xt_0) = \frac{i_0}{c} \int_0^{xt_0} f(\frac{t}{x})dt$$

By a simple change of the variable of integration,

$$\frac{i_0}{c} \int_0^{xt_0} f(\frac{t}{x})dt = x \frac{i_0}{c} \int_0^{t_0} f(t')dt'$$

Or, $v_C(nxT + xt_0) = xv_C(nT + t_0)$. This is the desired proportionality relationship which implies that under the stated assumptions, the signal level is independent of scan rate, with constant illumination. If this relationship were anything but linear, the diode D would become forward biased at different phase angles of the i(t) curve, depending on the scan rate, resulting in

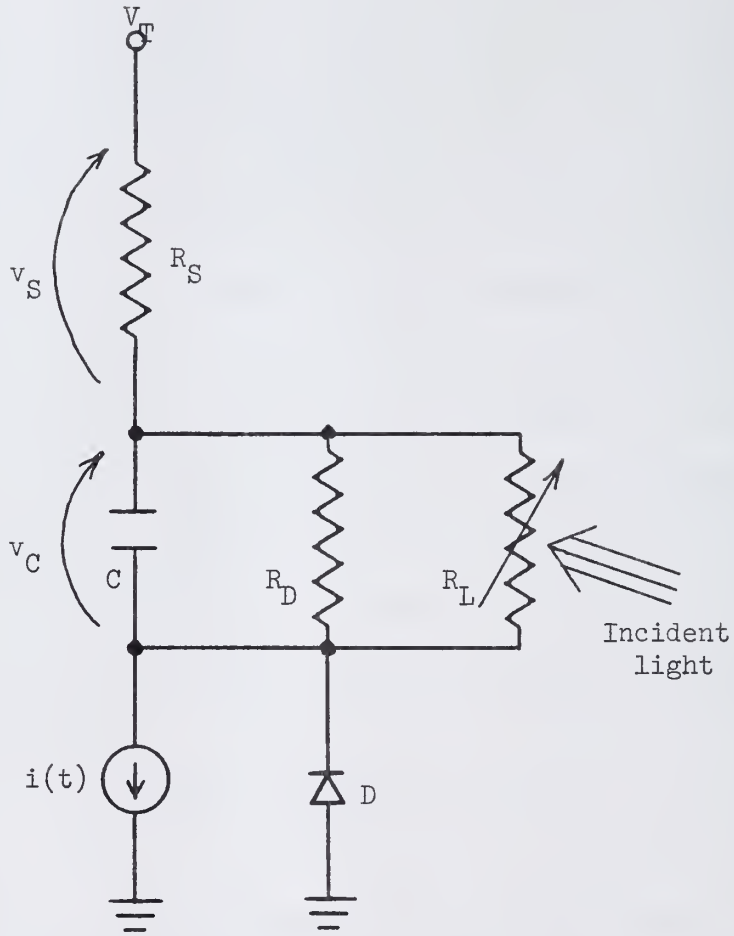


Figure 3.6.1.2 Complete Circuit for Each Element of the Target Surface

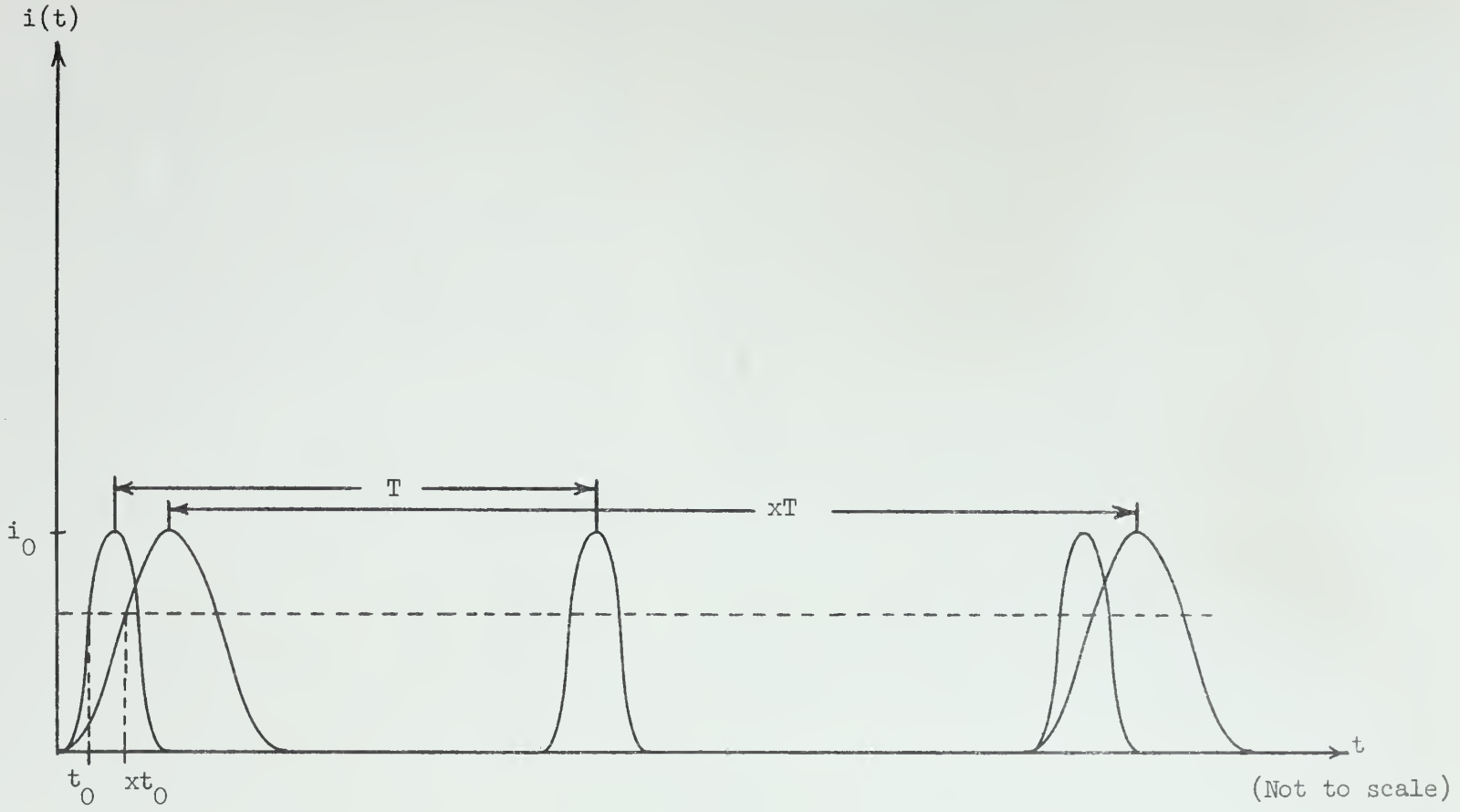


Figure 3.6.1.3 Beam Current at a Point as a Function of Time shown for a frame time of T seconds and for a frame time of xT seconds

different signal amplitudes. Figure 3.6.1.4, which shows the dependence of the signal amplitude on time t_0, perhaps clarifies this point.

A more detailed example will show the dependence of the signal amplitude on scan rate when certain of the above assumptions are not made. It is still perfectly reasonable to neglect the resistances R_D and R_L during the recharging process. In addition, the discharging and recharging processes will be treated as two separate events since the recharging time is so small compared to the corresponding frame time. Further, it will be assumed that diode D does, indeed, become forward biased sometime during recharging. In reality, this is not necessarily the case. The event that diode D does not become forward biased is one of the causes of the phenomenon known as picture lag.[15] Insofar as signal level is concerned, however, this case is of no interest; the signal voltage will always be $v_S(t) = i(t)R_S$, whose amplitude is i_0R_S regardless of scanning rate.

Although the beam spot current distribution is the error function, the function $f(x) = [1 + \cos(\xi)]$ is a very close approximation.[16] The latter distribution will therefore be employed in the details which follow. This waveform is illustrated in Figure 3.6.1.5. At this point a factor k is introduced for convenience. k is large number by which the frame time T is reduced to give the recharging period $(\frac{2\pi xT}{k})$. The origin will be taken at time $t = 0$, at which time the voltage across C has decayed from V_T to $V_T e^{\frac{-xT}{R_L C}}$, the initial voltage (V_0) across C when recharging commences. R_D is neglected during the discharging process since it is generally large compared to R_L. The signal voltage is simply

$$v_S(t) = i(t)R_S = \frac{i_0R_S}{2}[1 - \cos(\frac{kt}{xT})].$$

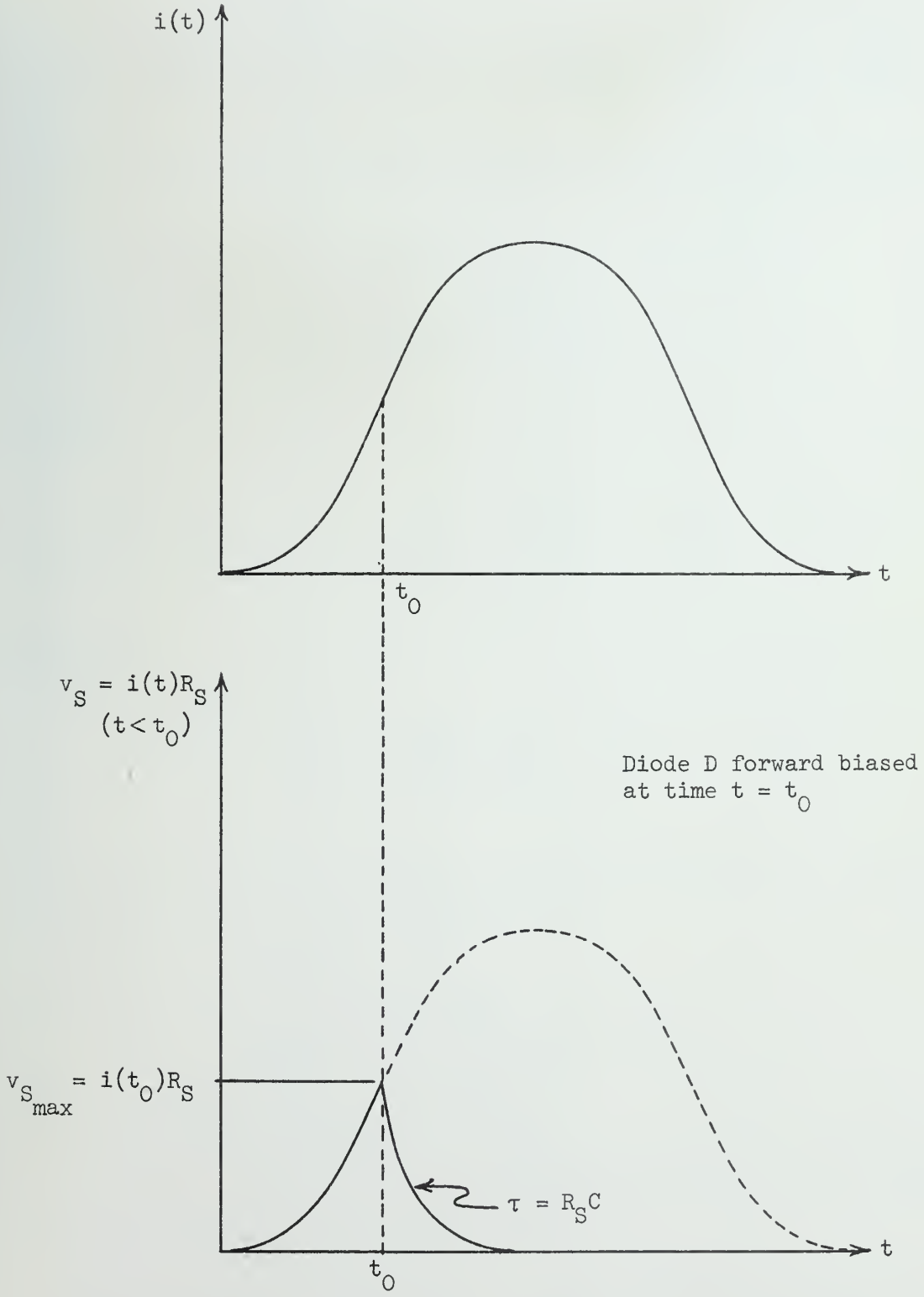


Figure 3.6.1.4 Waveforms Illustrating Derivation of Signal Amplitude

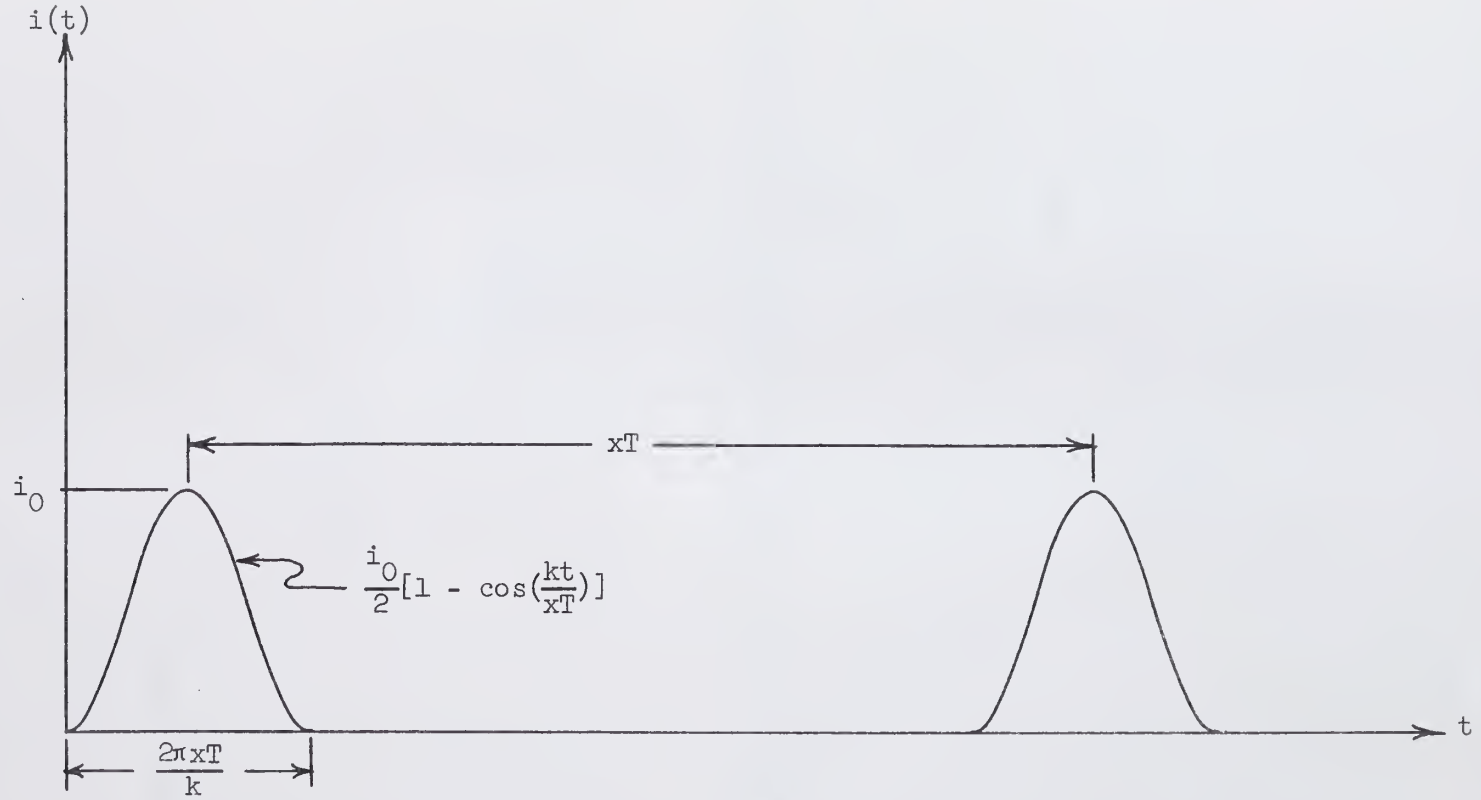


Figure 3.6.1.5 Beam Current at a Point Assuming the Distribution [1 + cos(ξ)]

The voltage by which v_C is increased at time t during the recharging period is

$$v_C(t) = \frac{1}{c}\int_0^t i(t)dt = \frac{i_0}{2c}\int_0^t [1 - \cos(\frac{kt}{xT})]dt = \frac{i_0}{2c}[t - \frac{xT}{k}\sin(\frac{kt}{xT})].$$

At time t_0, when diode D becomes foward biased, the following relation must obtain:

$$V_0 + v_C(t_0) + i(t_0)R_S = V_T$$

Therefore,

$$V_T e^{\frac{-xT}{R_L C}} + \frac{i_0}{2c}[t_0 - \frac{xT}{k}\sin(\frac{kt_0}{xT})] + \frac{i_0 R_S}{2}[1 - \cos(\frac{kt_0}{xT})] = V_T$$

Rearranging,

$$V_T(1 - e^{\frac{-xT}{R_L C}}) = \frac{i_0}{2c}[t_0 - \frac{xT}{k}\sin(\frac{kt_0}{xT})] + \frac{i_0 R_S}{2}[1 - \cos(\frac{kt_0}{xT})]$$

The solution of this transcendental equation determines time t_0, which in turn may be used to find the signal amplitude

$$v_{S_{max}} = v_S(t_0) = \frac{i_0 R_S}{2}[1 - \cos(\frac{kt_0}{xT})]$$

Notice that if $e^{\frac{-xT}{R_L C}}$ is replaced by its linear approximation, and the last term on the right is ignored, the equation becomes

$$\frac{2kV_T}{i_0 R_L} = \frac{kt_0}{xT} - \sin(\frac{kt_0}{xT})$$

the solution of which gives t_0 as a linear function of x. This implies that $v_{S_{max}}$ is independent of x, the result first predicted assuming linear storage and neglecting the signal voltage during the recharging process.

The numerical results of this analysis are displayed on the graph of Figure 3.6.1.6. Typical values were chosen for all the circuit elements. Values of t_0 were calculated for each integral value of x from 1 to 10. Each value of $v_{S_{max}}$ was then calculated and normalized. Also shown in Figure 3.6.1.6 are the linear storage approximation and the experimentally measured values of $v_{S_{max}}$.*

---

*The stray capacitance between the target and all other electrodes in the vidicon has been omitted in the entire preceding analysis. This capacitance is by no means negligible, amounting to something of the order of 5 or 6 picofarad. This, in conjunction with a resistance R_S = 50 kilohms, for example, results in a time constant of 250 or 300 nanoseconds. Although this has a drastic effect on the high frequency response of the television camera, ommission of the stray capacitance in no way invalidates the preceding results. The stray capacitance tends to average the voltage across R_S due to the current contributions from all the individual elements. This and the fact that the target surface is, in reality, a continuum accounts for the smooth nature of the video signal as the beam traverses areas of the target which are uniformly illuminated.

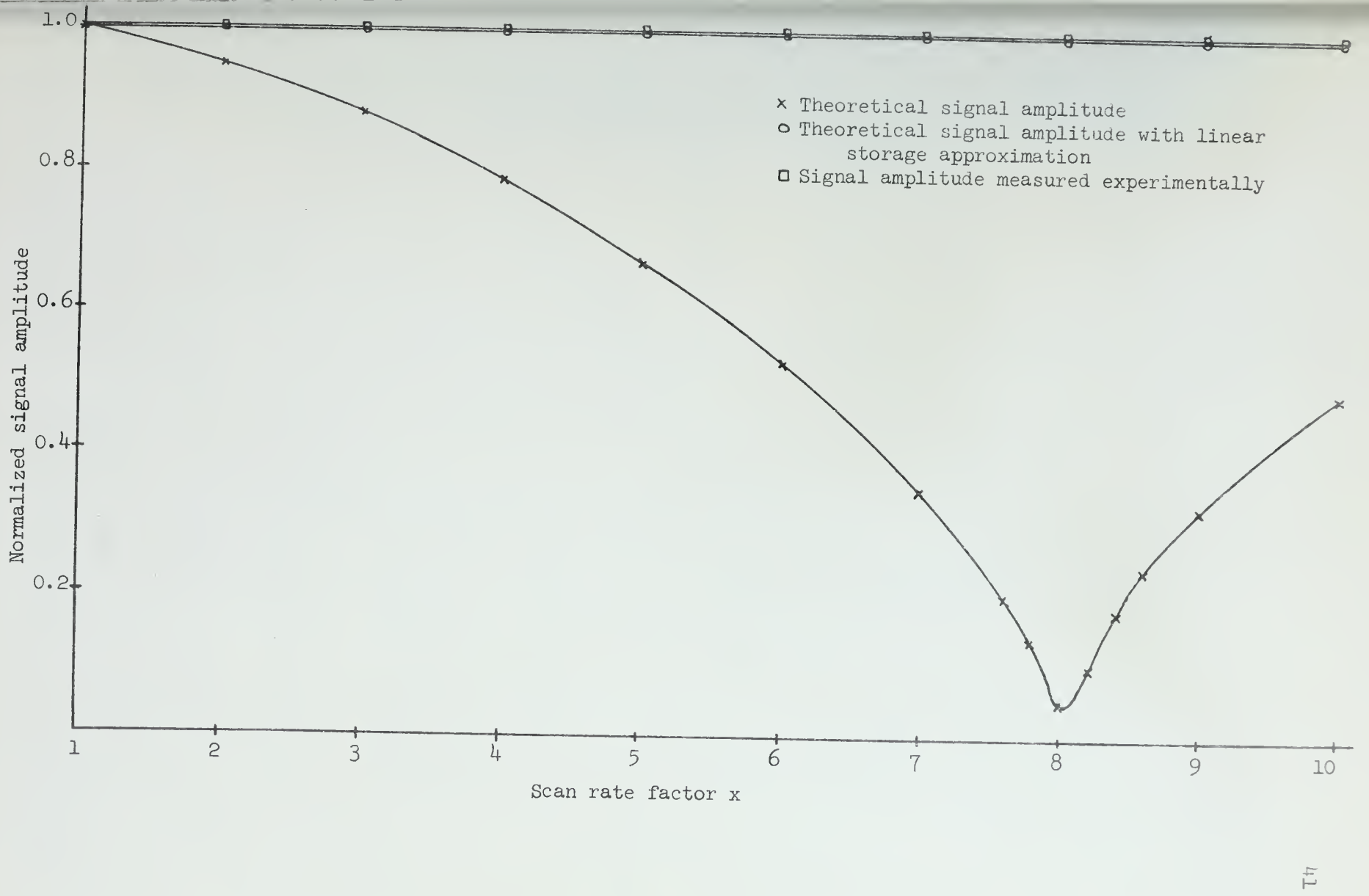


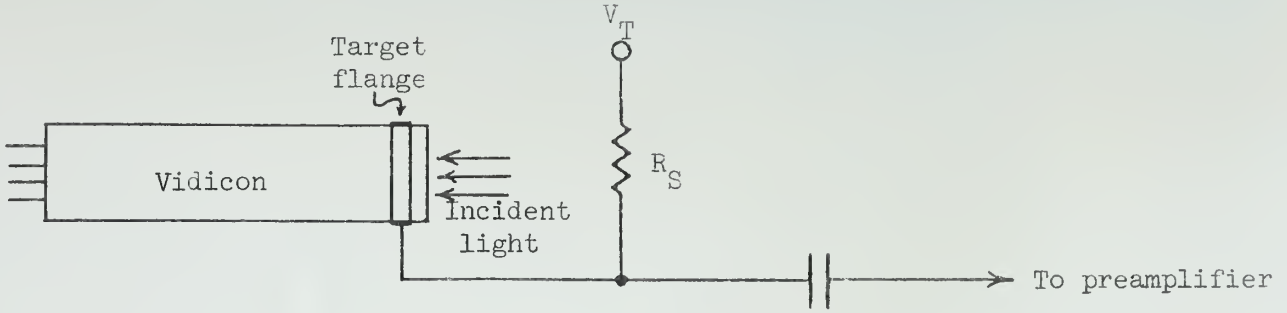
Figure 3.6.1.6 Normalized Signal Amplitude as Function of Scan Rate with Constant Illumination

3.6.2 Video Preamplifier

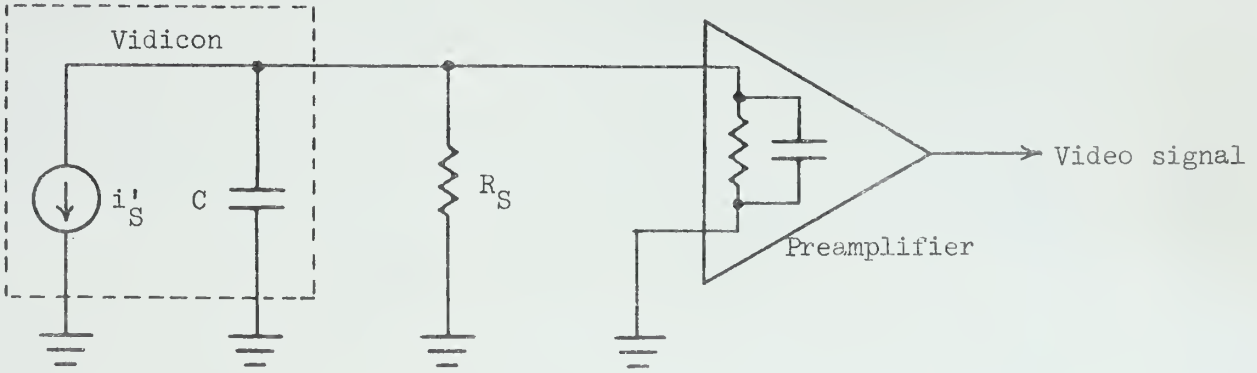
From the results of the preceding analysis, it was clear that some gain control might be required, despite the fact that to a first approximation the signal level was found to be independent of scan rate with constant illumination. A gain control facility was therefore provided in the event that such control proved necessary. Since it would be prohibitively costly to implement 64 different values of gain corresponding to the 64 different scan rates, nine or ten ranges of scan rates were selected, each corresponding to a single value of signal gain. The gain range discriminator was designed to catagorize each scan rate in the appropriate range. Upon selection of a range, the gain of the preamplifier was set accordingly.

Figure 3.6.2.1 is a simplified diagram of the vidicon-preamplifier circuitry. The vidicon is now considered to be equivalent to a current source $i'_s(t)$ paralleled by the stray capacitance C_S. The gain is adjusted by varying the value of R_S, rather than by controlling the gain in latter stages of the preamplifier. This technique provides a control of the noise level by reducing the high frequency response as R_S is increased for lower scan rates. By increasing R_S, the $R_S C_S$ time constant is increased, where C_S is the stray capacitance between the target mesh and all other electrodes in the vidicon. Since the majority of the noise originates as thermal noise in R_S, this decrease in frequency response offsets the increasing noise level which varies as the square root of R_S.

The input resistance R_S is controlled by using a field effect transistor as a voltage controlled resistor. The voltage, in turn, is controlled by a resistor divider composed of a standard resistor and a Hewlett-Packard photocell-lamp combination. This arrangement offers excellent isolation between



Vidicon circuit



Small signal equivalent of vidicon circuit

Figure 3.6.2.1 Simplified Diagram of Vidicon-Preamplifier Circuit

the controlling mechanism and the input resistance R_S, an important consideration at such low signal currents. This circuit is shown in Figure 3.6.2.2. A feedback signal is returned to the gain control circuit from the preamplifier in order to bootstrap the gate and null the effect of the gate-to-drain capacitance.

A field effect transistor is used at the input of the preamplifier for its high input impedence characteristics. This prevents attenuation of the already small signal level. Figure 3.6.2.3 shows the preamplifier circuit. Here Q_2, used as an emitter follower, bootstraps the source and drain through C_1 and C_2, respectively, thus eliminating the effect of the gate-to-source capacitances. In a similar manner, the collector of Q_2 is bootstrapped through C_3. The input capacitance to the preamplifier circuit was measured at approximately 0.8 picofarad. The input resistance is well over 10 megohms.

A combination of series and shunt peaking is employed in stages Q_5 and Q_6.

In order to enhance television picture detail, conventional television preamplifiers employ a peaking stage to boost the high frequency response. This technique was employed in this preamplifier design, though not to the extent that it nulled the noise reduction effect described above. Here an additional complexity arose due to the variable gain feature of the preamplifier. As the upper frequency limit falls off with increasing R_S, as discussed above, the peak must shift accordingly. Thus a different pole-zero combination is switched into the circuit for each of the gain settings. This is shown in the emitter circuit of Q_7 in Figure 3.6.2.3. The networks switch simultaneously with the different values of R_S.

The voltage gain of the preamplifier is approximately 40 decibels.

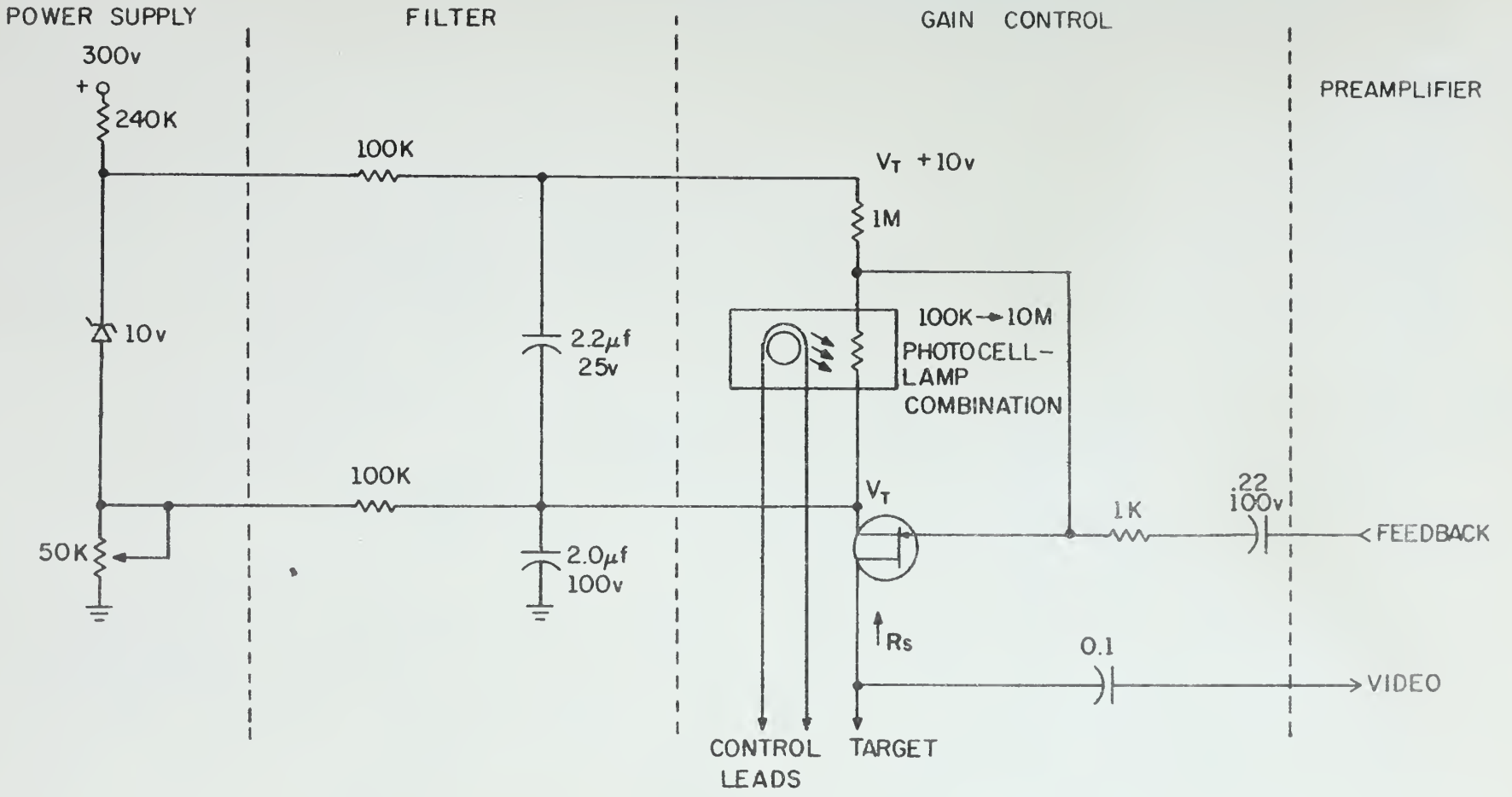


Figure 3.6.2.2 Gain Control Circuit

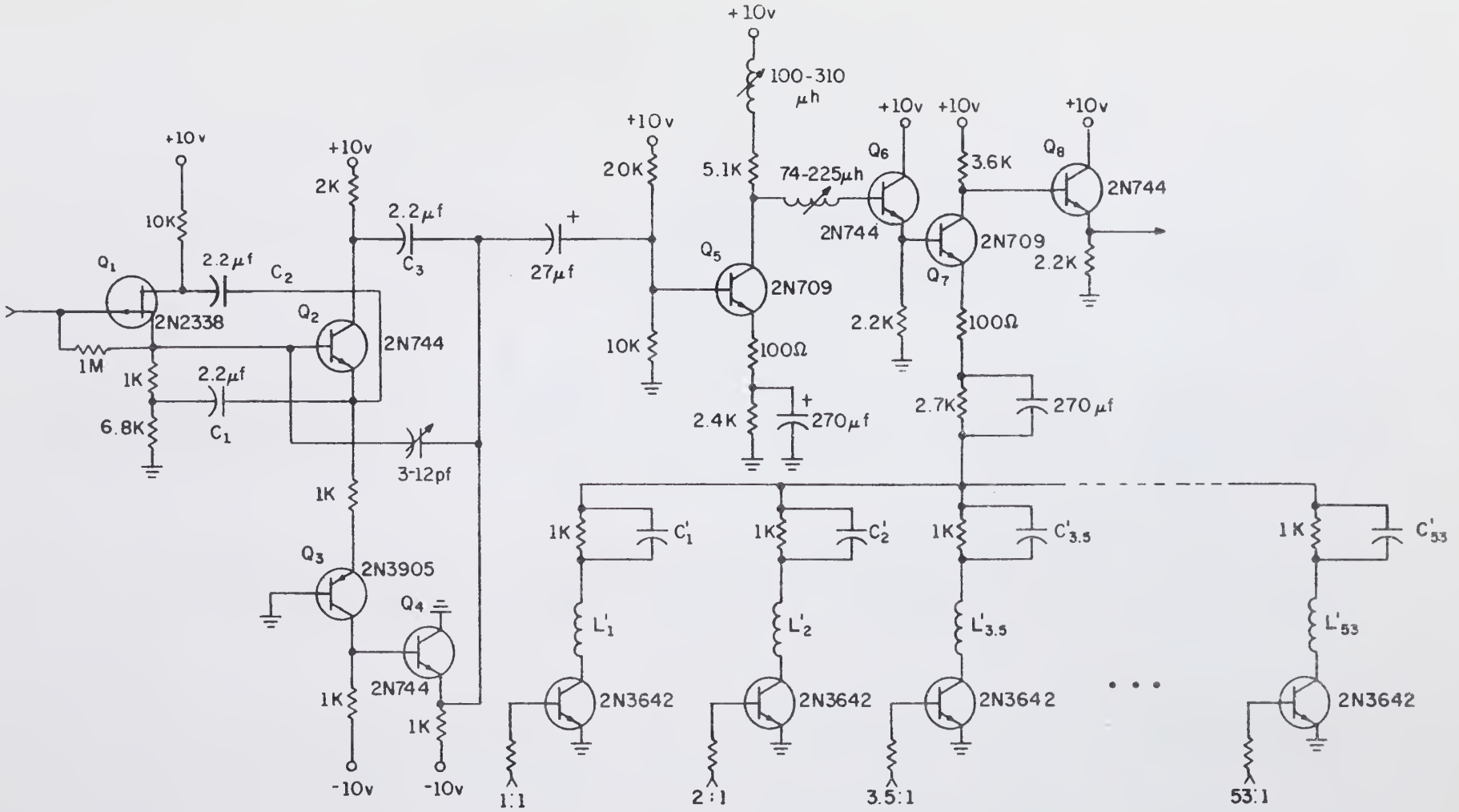


Figure 3.6.2.3 Video Preamplifier

3.6.3 Range Discriminator Circuit

Each scan rate was catagorized into one of nine different ranges, each range corresponding to one of nine different preamplifier gain and filter values. An analytic approach was extremely useful as a basis for selecting the different ranges. This derivation is outlined in the appendix along with a typical example.

It was immediately obvious that an analog, rather than digital approach was far better suited to the classification of 64 different scan rates among nine ranges. Decoding 64 different possibilities of a 7-bit binary number digitally would have been a formidable task, indeed. Instead, an analog conversion was performed, and the resulting analog number was classified in the manner of Figure 3.6.3.1. Each pair of differential amplifiers were connected in such a way that each responded if the analog voltage fell within its window. The numbers corresponding to the first two windows, being very simple binary numbers, were coded digitally while the analog technique was applied to the remaining ranges.

The digital output of each pair of amplifiers controls a simple transistor switch. This, in turn, activates one of nine different LC filters in the preamplifier and generates one of nine possible values of current in the photocell-lamp gain control facility. An attractive feature of this scheme is that the integral nature of the scan rates allows the windows to be chosen such that no overlap occurs, and the scan rate numbers will always fall within one and only one window.

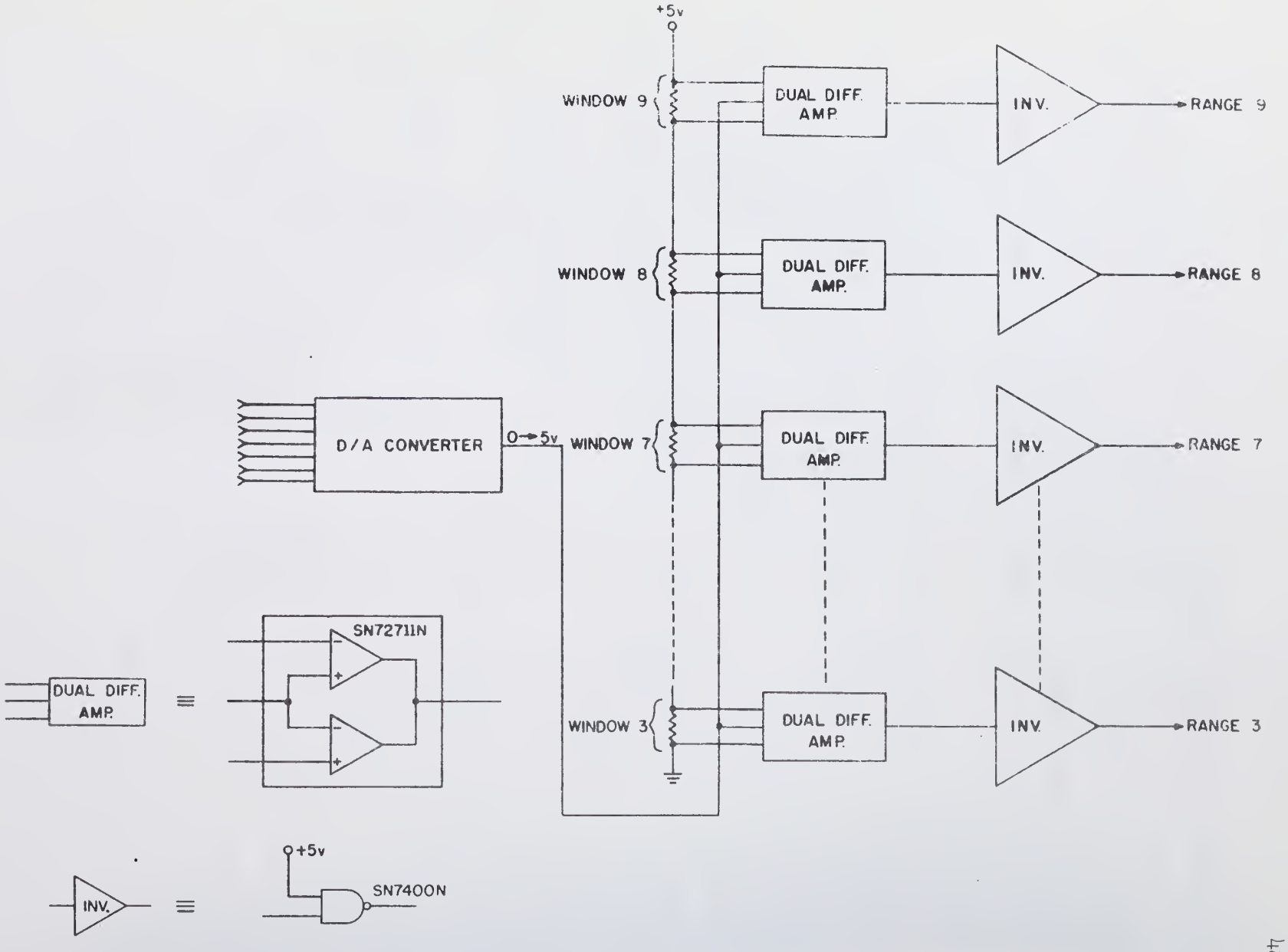


Figure 3.6.3.1 Gain Range Discriminator

3.6.4 Vidicon Protection in the Event of Scan Failure

The problem of vidicon protection was compounded by the variable scan rate nature of the system. In a single scan rate system, slope detection applied to the horizontal voltage ramp is a simple and useful approach. In such a scheme, when the voltage amplitude corresponding to the first derivative of the ramp falls below a predetermined value, a blanking voltage is applied to the vidicon to prevent burning the target. This technique, with several simple modifications, was applied to the case of the variable rate horizontal scan. The deflection failure detector shown in Figure 3.6.4.1 is composed of two differential amplifiers together with their related components. The .001 microfarad capacitor and the 10 kilohm resistor tied to ground constitute the differentiating network. The differentiated voltage is compared with a reference via the first differential amplifier. When the threshold is exceeded, an output pulse is applied to the logic elements and the following integrating network. These elements prevent the circuit from reacting during horizontal retrace, or that portion of the ramp with negative slope. The protection circuit may blank the cathode of the vidicon only when the blanking input is a logical "1". The derivative of the horizontal ramp appeared to be an ideal source for extracting the blanking signal directly. Unfortunately, however, the time delay due to the differentiating network could not be tolerated, hence the blanking signal was derived at the horizontal ramp generator.

The stair-step nature of the vertical ramp dictated a different scheme for protection of the vidicon. The nine binary inputs to the D/A converter, which produce the vertical deflection waveform, are monitored collectively. Each input is applied to a differentiating network, and the combined output is compared with the horizontal blanking signal. If at least one of the binary inputs changes state, in either direction, a flip-flop will

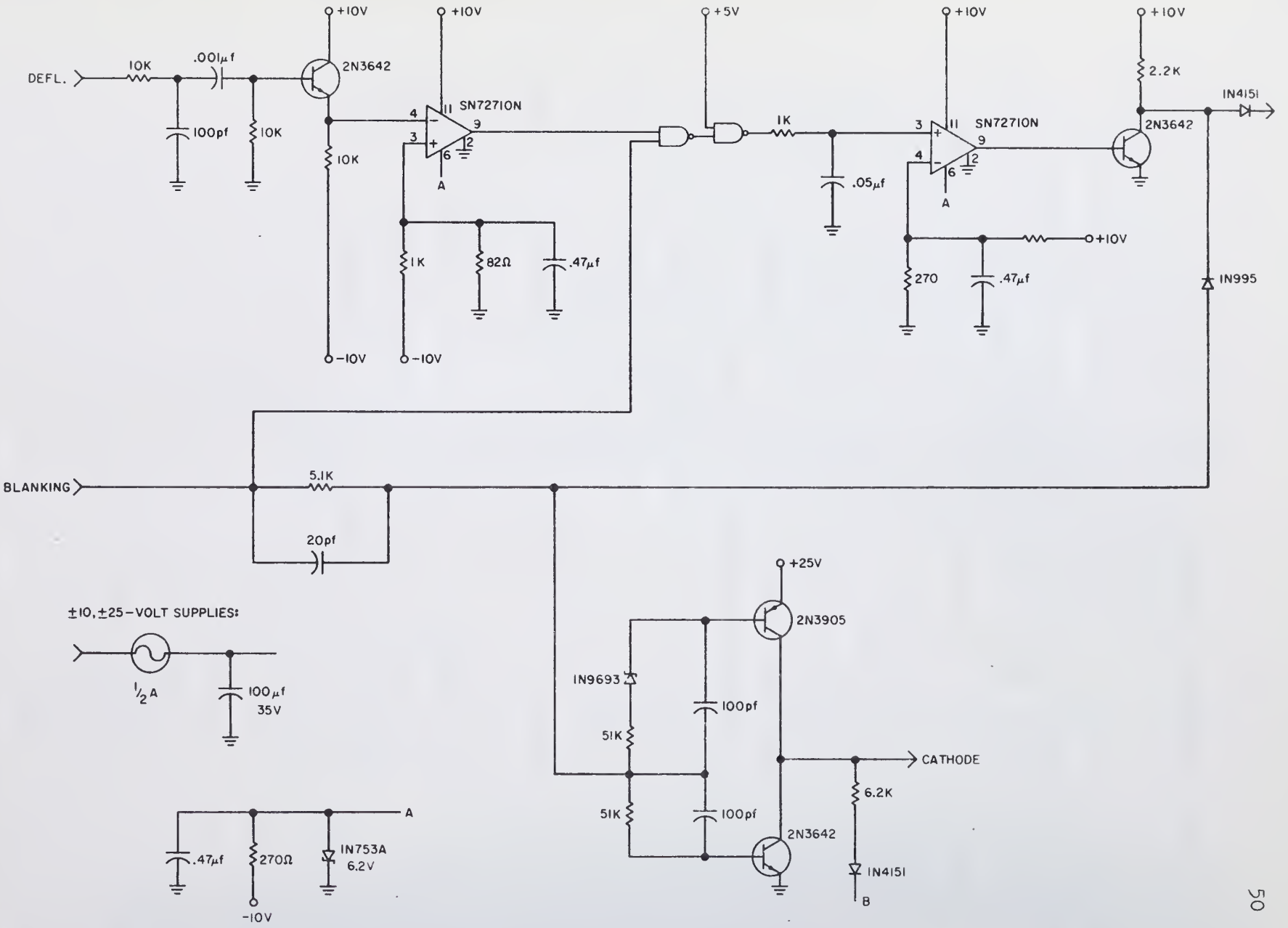


Figure 3.6.4.1 Horizontal Deflection Failure Detector

be reset. If no change occurs, indicating that the vertical waveform has not changed between two successive scans, the flip-flop will not be reset, and the cathode of the vidicon will remain blanked. Figure 3.6.4.2 shows the complete circuit. This scheme is obviously not infallible, for the fault could lie in the D/A converter. A trade-off between complexity and probable failure rate resulted in the choice of this scheme.

3.6.5 Deflection Amplifiers

Due to the shifting nature of the television raster, direct-coupled deflection amplifiers were required to drive the plates of the electrostatic vidicon tube. The specifications called for 30 volts peak-to-peak deflection voltage per plate with an average voltage of 225 volts. An inverting and a non-inverting amplifier circuit were designed using operational amplifiers and high voltage transistors as shown in Figure 3.6.5.1. The signal outputs were returned through feedback resistors to the inputs. One such pair of amplifiers is used to drive the horizontal plates, and an identical pair to drive the vertical plates. The linearity and response of the amplifiers are excellent over the entire range of scan rates.

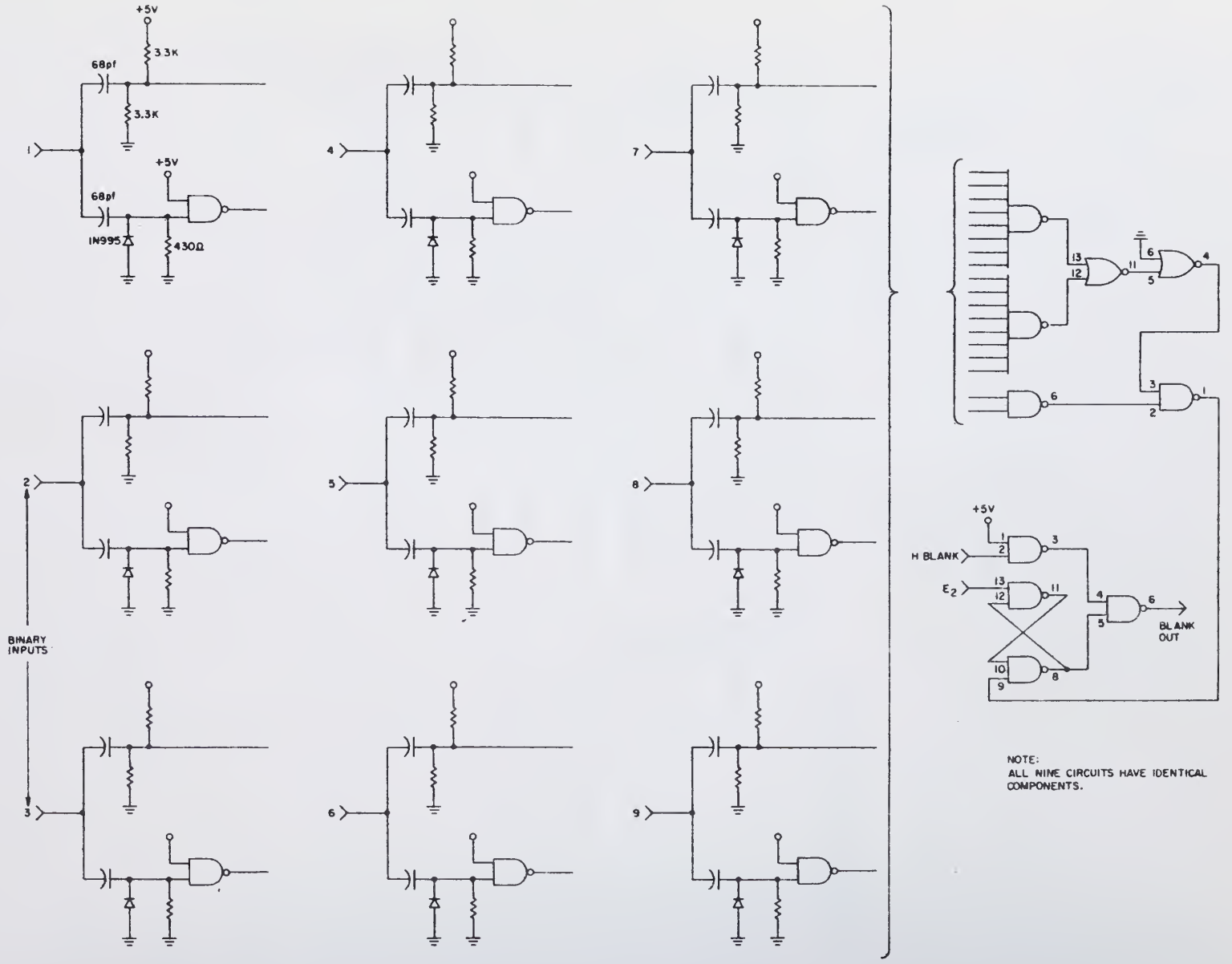


Figure 3.6.4.2 Vertical Deflection Failure Detector

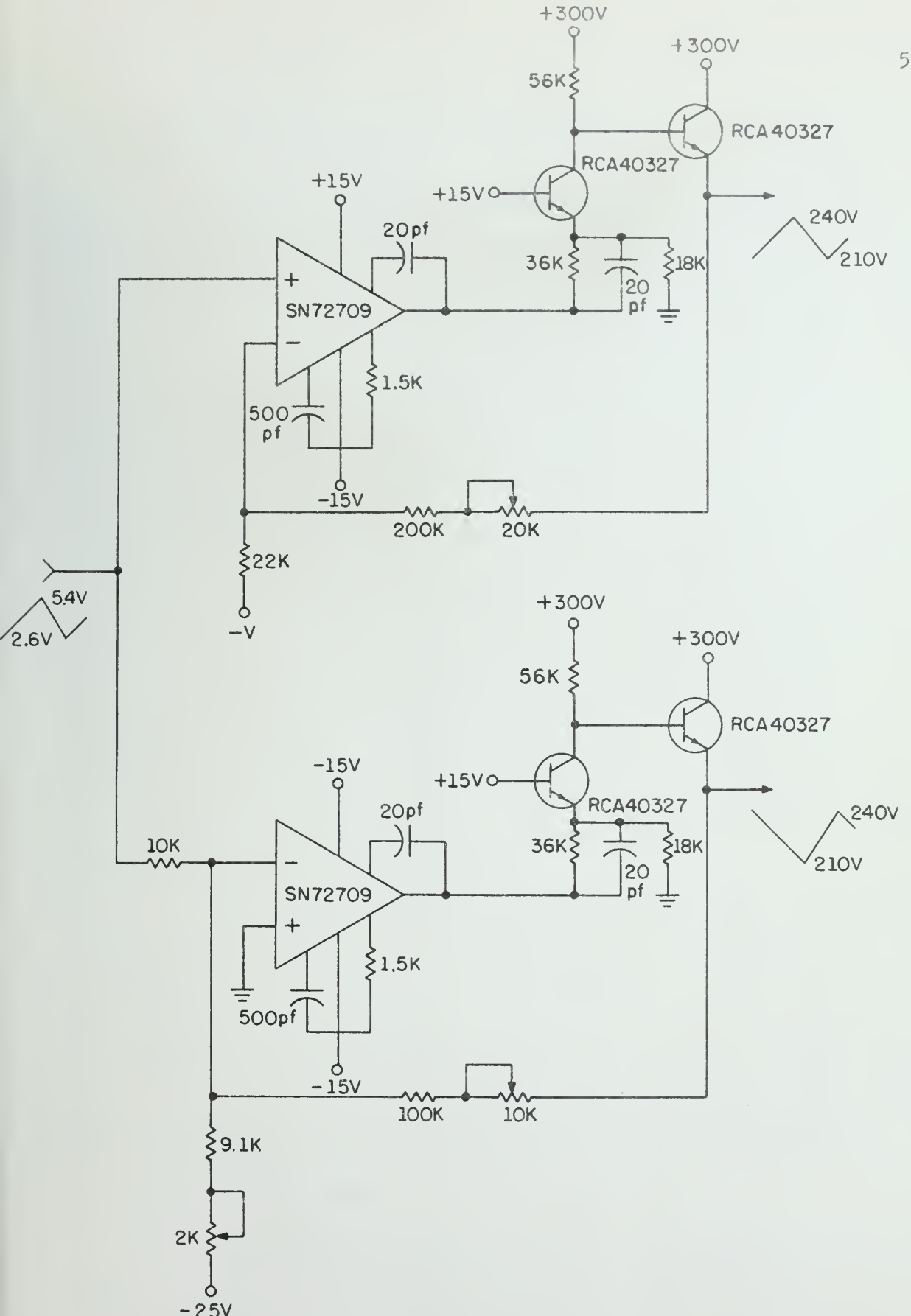


Figure 3.6.5.1 Deflection Amplifiers

4. CONCLUSION

The success of the VISTA system was limited to a large extent by the variable persistence oscilloscope. Although the persistence control performed admirably over the useful range of scan rates, the device was incapable of displaying shades of gray between the black and white extremes. The tube is essentially a bistable storage tube, and as such is useful for displaying printed matter only. Any attempt at displaying a multishade picture resulted in an enhancement of those levels above the bistable brightness threshold, and a fading away of those levels below the threshold. Although the manufacturer claimed that four gray levels could be resolved, these levels were indistinguishable in the presentation of typical television pictures. In spite of the inability to display gray levels, however, the device worked quite well. The presentation of black and white pictures or printed matter clearly demonstrated the usefulness and success of the variable persistence technique. An optimum adjustment exists beyond which the picture will begin filling in (this phenomenon is known as picture "bloom"), and below which the bar drift effect will be noticeable. Of course at high persistence levels the inability to transmit picture motion becomes more pronounced due to the longer decay time. This effect predominates over the inability to transmit picture motion due to the reduced scan rate. Presumably, however, insufficient motion occurs at such reduced rates to warrant a faster decay rate.

The bandwidth compression ratio corresponding to the least acceptable picture quality was in the vicinity of eight-to-one. Again, the persistence feature was the limiting factor. The degree of persistence required to null the bar drift effect beyond this ratio caused the picture to fill in, or bloom. It was found that a single setting of the persistence control sufficed for all scan rates up to the eight-to-one reduction.

Strangely enough, the television camera was not the limiting component as had originally been anticipated. In fact, satisfactory video signals were derived over the entire range of sixty-four different scan rates! Even more surprising was the fact that no gain control was required over this extreme range. In view of the detailed analysis in section 3.6, the author concludes that the estimate of the capacitance value per element was incorrect in spite of the reliable source of information.[15] The reason for this conclusion was the persistence characteristics, or more precisely the signal decay characteristics associated with the vidicon upon removal of the light excitation. Evidently the elemental capacitances are not fully recharged as the beam strikes each element. This, of course, is one cause of picture lag as mentioned previously. In this case the signal level is a function only of the beam current, and hence is not a function of frame rate assuming constant illumination. The capacitance associated with each element must be larger than anticipated to substantiate this result. This would also lead to a more linear storage since the exponent of the discharging relationship varies as 1/C. This lends further credence to the above argument.

A second observation is consistent with the incomplete recharging of the elemental capacitances. An acceptable picture was derived after scanning only one complete frame at any one of the different scan rates. Thus it is sufficient to scan a single frame in each of the slow and fast modes, alternately. This implies that the information change may be monitored more often since it is not necessary to allocate several frames for steady state operation of the vidicon in the slow scan mode.

The most acceptable interlace pattern was an alternate up and down shift of the raster. This pattern resulted in the maximum amount of raster motion, thus reducing the bar drift effect most successfully. The exact

starting line sequence appeared not to matter as long as the raster shifted up and down alternately in large steps. The following two starting line progressions were equally effective and gave the best quality pictures: 1, n, 2, n-1, . . ., n/2, n/2+1 and n/2+1, n/2, n/2+2, n/2-1, . . ., n-1. The use of two counters in the alternate mode was noticeably better than the use of either counter alone. A comparison between the n-to-one interlace scheme and the line sequential scheme left no doubt as to the effectiveness of the former. At any one of the reduced scan rates, the flicker problem rendered the line sequential pattern completely unacceptable as anyone might expect. Ideally, a completely random interlace scan would probably be the most desirable type of interlace pattern, though the dynamic characteristics of the vidicon preclude such an application. A pseudo-random type dot scan has been dealt with quite extensively,[10] but the complexity of the synchronization signal requires a rather elaborate decoding process. Here the variable interlace scheme enjoys quite an advantage, though it does not approach the degree of randomness associated with the pseudo-random dot scan. The required synchronization signals add little complexity to the commercial television scheme since the variable scan is a simple extension of the standard two-to-one interlaced scan.

The usefulness of the variable interlaced scheme depended to some extent on the nature of the picture being displayed, as well as on the scan rate. The display of regular geometrical figures resulted in objectionable moiré patterns due to the regular, repetitive nature of the interlaced sequence. Picture detail in the vertical direction became obscured as some horizontal lines faded while others were being scanned. Combined with the variable persistence feature, however, a high quality picture was obtained at compressions up to eight-to-one with no deterioration due to moiré patterns or loss of detail. It was concluded, then, that both the alternating up and down raster interlace

and the variable persistence feature were essential in obtaining high quality pictures at reduced scan rates.

At the time of this writing, a rather different approach to the variable persistence display is being pursued which will adequately present a multishade television picture. This idea was set forth by Sylvania, Division of General Telephone and Electronics Company, and is an extension of the single gun color tube principle. In this scheme, two different phosphor layers are deposited on the CRT screen, and a variation in the accelerating potential alters the degree of penetration of the electron beam in the phosphor coatings. This provides a continuous color variation from one color phosphor to the other. In the VISTA system application, the phosphor coatings would be of the same color, but possess different decay characteristics. Thus the persistence could be controlled continuously between the two extremes.

The detection of information changes between successive television frames and the automatic selection of a bandwidth compression ratio was a successful venture, though slightly more complex than was initially anticipated. An unexpected problem was the large measure of cross talk between channels of the video disc recorder during the READ and WRITE operations. The cross talk was so excessive, in fact, that the sequential video switching scheme between channels had to be altered. In the final design, the READ and WRITE operations were sequenced such that the two operations were never performed simultaneously. This entailed the use of an additional frame period at the end of each fast scan mode. This also permitted the use of two tracks instead of three with a vacant track between the two to further isolate the channels during the erase operation. These measures successfully inhibited any noticeable cross talk.

Due to the nature of the magnetic disc and the desirability of storing large shaded picture areas instead of fine details alone, the disc was used in a "chopped" video mode. The result was an amplitude modulated 3MHz signal which had to be demodulated before a comparison beteen video signals could be performed. A demodulator was thus designed and built for this purpose which consisted of a full-wave rectifier and peak-follower circuit.

An accurate control of the video signal levels and amplitudes was required for a valid comparison between successive frames. Any unbalance was integrated by the compare and hold circuit and resulted in a false indication of the information change. Many signal level restoration and gain control circuits were thus required, particularly since the WRITE signal amplitudes required by the disc differed for the two channels, and the video signals read from the disc also differed.

In general, the system functioned rather well in the automatic mode. Any object waved in front of the camera, for example, resulted in the selection of a larger bandwidth for the video signal, the exact selection depending on the motion and size of the object.

APPENDIX

A.1 Disc Video Control

The mechanism by which the video signal emerging from the camera is simultaneously stored and compared with the previously stored frame is the disc video control. The video signals must be shunted between three tracks of the disc recorder in order to read, write and erase simultaneously during each fast scan mode of operation. A newly erased track accomodates the video signal during the next fast scan, at which time a different track will be erased. Similarly, a different track will be written upon. Figure A.1.1 illustrates the disc video control which comprises a modulo 3 counter, a decode section and a series of video gates. The modulo 3 counter changes state each time the system reverts to the fast scan mode. During this time the decode AND elements are activated. Depending on the particular count, one each of the erase, read and write gates will open to permit passage of the corresponding signals. Each time the count changes, a different set of three gates will open, thus permuting the read, write and erase signals among the three tracks.

A.2 Analog-to-Digital Converter

The analog delta density signal is converted to a digital signal for use by the horizontal ramp generator and other subsystems. A six-bit conversion is required for selection of one out of 64 possible scan rates.

Figure A.2.1 is a simplified block diagram of the A/D converter. A trigger signal activates the clock for six complete periods which enables the ring counter to complete one full cycle. As each D-type flip-flop is strobed, beginning with the most significant bit, the resulting analog voltage at the output of the D/A converter is compared with the analog delta density input signal. If the analog input exceeds the D/A output, the D-type flip-flop remains in the "1" state. If the D/A output exceeds the analog input a logical

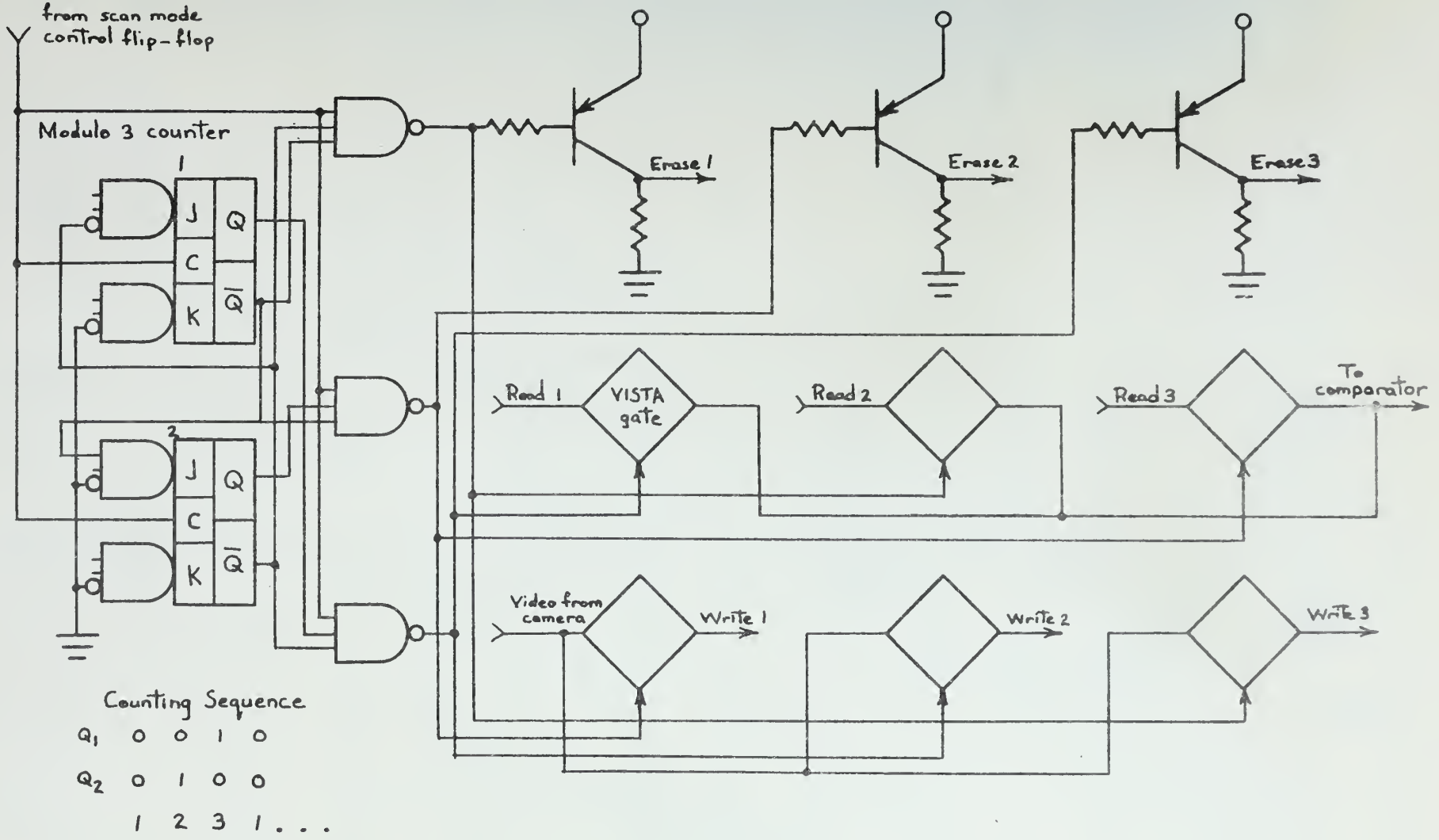


Figure A.1.1 Disc Video Control

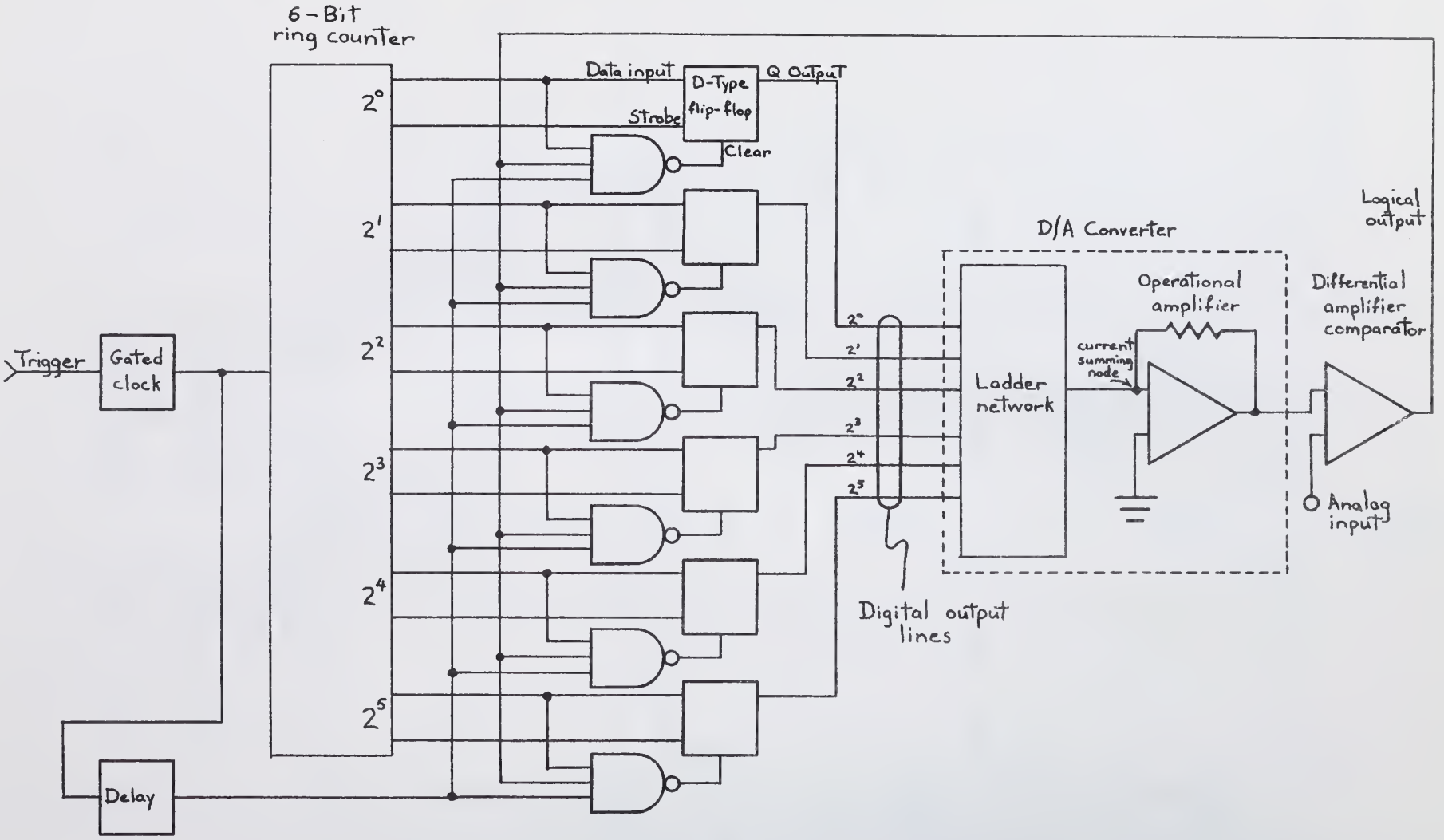


Figure A.2.1 Analog-to-Digital Converter

"1" appears at the output of the differential comparator which clears the Q output of the D-type flip-flop to a logical "0". A similar comparison is made for each of the less significant bits, in descending order, during each successive clock period. When all six D-type flip-flops have been so addressed, the digital conversion appears on the output lines shown in Figure A.2.1.

A.3 Partitioning the Scan Rates into n Ranges

Having calculated the desired gain for each of the 64 possible scan rates, an algorithm was developed for partitioning these scan rates into n ranges, $n < 64$, to economize and simplify the circuitry. Obviously this results in some error, since only one scan rate in each of the n ranges will correspond exactly to the gain value chosen for all the scan rates within that range. Clearly, the greater n is, the closer the scan rates $1/xT$ will come to their corresponding gains $G(x)$ (recall that T is the fastest frame time, x is the factor by which the fastest scanning speed is reduced), and the smaller will be the error.

For the purposes of the derivation, Figure A.3.1 presents a hypothetical gain versus scan rate factor curve illustrating the partitioning procedure. For any x_j, $j = 1, 2, \ldots, n$, the band corresponding to the coordinate distance $2\Delta x_j$ will be

$$G(x_j + \Delta x_j) - G(x_j - \Delta x_j) = 2 \left.\frac{\delta G}{\delta x}\right|_{x = x_j} \delta x_j$$

Summing these increments,

$$G_{max} - G_{min} = 2 \left.\frac{\delta G}{\delta x}\right|_{x=x_1} \Delta x_1 + 2 \left.\frac{\delta G}{\delta x}\right|_{x=x_2} \Delta x_2 + \ldots + 2 \left.\frac{\delta G}{\delta x}\right|_{x=x_n} \Delta x_n = 2 \sum_{j=1}^{n} \left.\frac{\delta G}{\delta x}\right|_{x=x_j} \Delta x_j$$

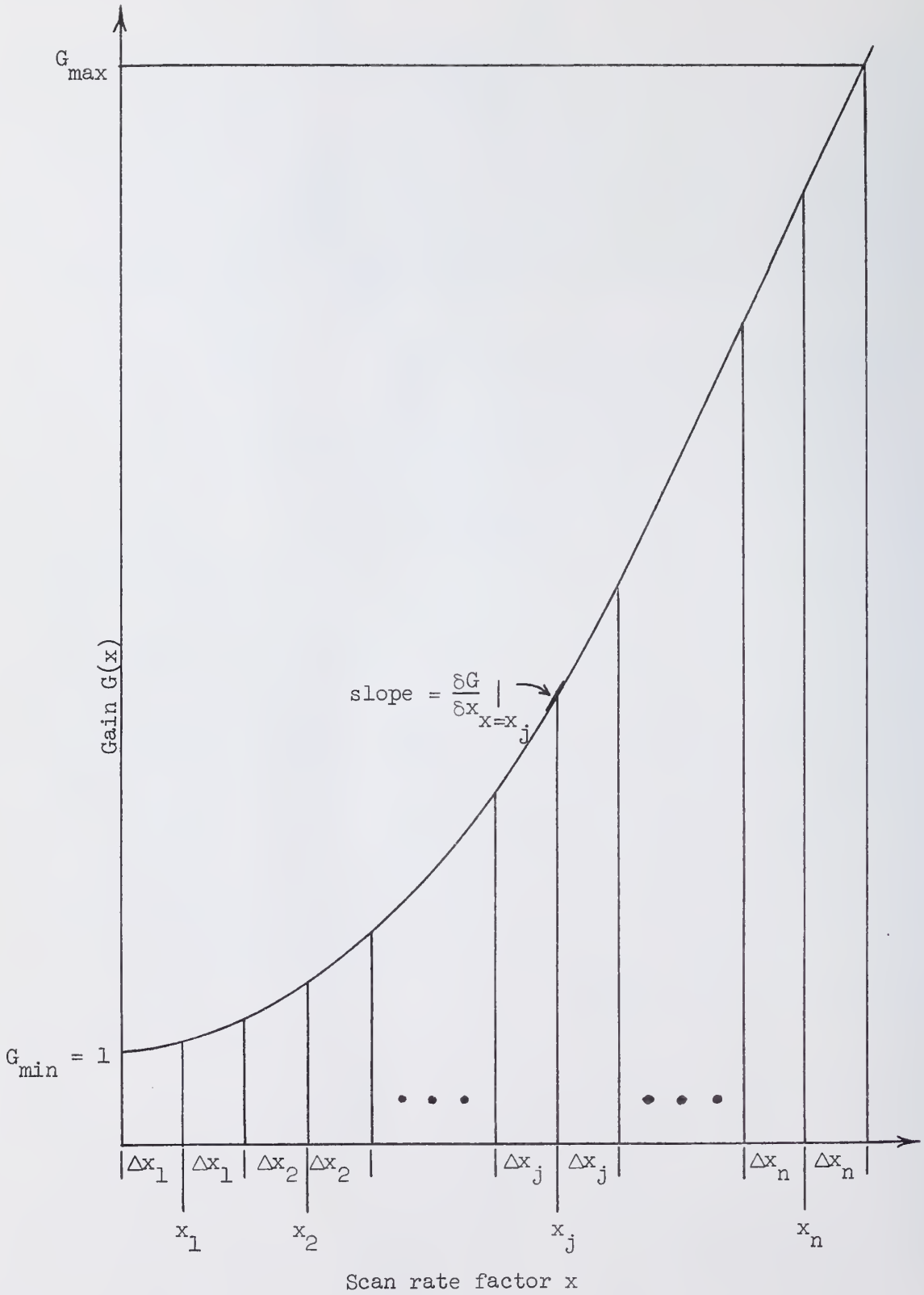


Figure A.3.1 Partitioning Procedure Applied to a Hypothetical Gain Curve

A convenient criterion to apply to the partitioning procedure is that the maximum per cent error in gain not exceed some value δ for every one of the n ranges. Thus,

$$\delta = \frac{1}{G(x_1)} \left.\frac{\delta G}{\delta x}\right|_{x=x_1} \Delta x_1 = \frac{1}{G(x_2)} \left.\frac{\delta G}{\delta x}\right|_{x=x_2} \Delta x_2 = \cdots = \frac{1}{G(x_n)} \left.\frac{\delta G}{\delta x}\right|_{x=x_n} \Delta x_n$$

Therefore,

$$G_{max} - G_{min} = 2\delta \sum_{j=1}^{n} G(x_j)$$

A useful recursion relation is the following:

$$G(x_j) + \delta G(x_j) = G(x_{j+1}) - \delta G(x_{j+1})$$

Therefore,

$$G(x_j) = \frac{1 - \delta}{1 + \delta} G(x_{j+1})$$

Letting $\gamma = \frac{1 - \delta}{1 + \delta}$, $G(x_j) = \gamma G(x_{j+1})$. An additional relationship now follows:

$$G(x_{j-k}) = \gamma^k G(x_j)$$

Substituting this expression, the series becomes

$$G_{max} - G_{min} = 2\delta(G_1 + G_2 + \ldots + G_n)$$

$$= 2\delta(\gamma^{n-1}G_n + \gamma^{n-2}G_n + \ldots + \gamma G_n + G_n)$$

$$= 2\delta(\gamma^{n-1} + \gamma^{n-2} + \ldots + \gamma + 1)G_n$$

where $G_1 = G(x_1)$, $G_2 = G(x_2)$, . . ., $G_n = G(x_n)$. The sum of this geometric series is

$$(\gamma^{n-1} + \gamma^{n-2} + \ldots + \gamma + 1) = \frac{1 - \gamma^n}{1 - \gamma}$$

Therefore,

$$G_{max} - G_{min} = 2\delta \frac{1 - \gamma^n}{1 - \gamma} G_n$$

G_n may be expressed in terms of G_{max}:

$$G_n = \frac{G_{max}}{1 + \delta}$$

Substituting this expression,

$$1 - \frac{G_{min}}{G_{max}} = \frac{2\delta}{1 + \delta} \frac{1 - \gamma^n}{1 - \gamma}$$

Since $\frac{2\delta}{1 + \delta} = 1 - \gamma$, the expression above reduces to

$$\gamma^n - \frac{G_{min}}{G_{max}} = 0$$

G_{min} is unity, so the final expression is

$$\gamma^n - \frac{1}{G_{max}} = 0$$

Thus it suffices to choose the desired number of ranges n from whence follows the per cent error δ and the range boundaries. The following example will illustrate the usefulness of these results.

Consider the linear gain function G = x. Ten ranges represent a reasonable yet not extravagant number of circuits. For n = 10 and $G_{max} = 64$, $\gamma = 0.66$. Therefore, $\delta = 25.4$ per cent maximum error. $G_{10} = \frac{G_{max}}{1 + \delta} = 51.0$. $G_\gamma = \gamma G_{10} = 33.7$, etc. Using the G(x) relationship, the scan rates within each range may now be calculated.

A.4 Steady-State Error Correction Applied to Horizontal Ramp Generator

An inherent property of the horizontal ramp generator, as pointed out in section 3.2, was its ability to correct for sudden or spurious displacements of the ramp voltage. A second type of error encountered is a steady state voltage error in the ramp amplitude. This may arise due to temperature effects on the constant current charging or discharging sources, as variations in the capacitance values, leakages or any other such slowly changing malfunction. A rather attractive scheme was developed for eliminating any voltage error within several ramp periods. Before departing on another analytic adventure, however, it should be pointed out that this error correction scheme was never actually implemented. Although a small error was detected, it was not sufficiently large to necessitate the use of an elaborate correction circuit. Nevertheless, the successful theoretical aspects of the scheme warranted a

description of the circuit and its effect upon the ramp voltage in the event of a hypothetical error. The outstanding characteristics of the scheme is its ability to cope with and correct an error almost instantaneously.

The basic idea is the detection of the voltage error by comparison of the peak ramp voltage with a reference, and the subsequent generation of a charging error current δI_0. δI_0 is a constant current which is added to the ramp charging current. At the conclusion of every horizontal line the ramp voltage is sampled in this manner, and the error currents generated are $(\delta I_0)_1$, $(\delta I_0)_2$, . . ., at the end of the first period, second period, and so on respectively. $(\delta I_0)_j$ is proportional to the voltage error at the end of the jth ramp period. Finally, as the error converges to zero the total charging current converges to $I + (\delta I_0)_1 + (\delta I_0)_2 + \ldots = I + \delta I_0$. Figure A.4.1 shows the bare essentials for implementing this correction scheme. The new error current for each cycle is derived during the previous retrace period and generated commencing with the beginning of the positive going ramp. The analog adder shown in Figure A.4.1 insures that the new error current adds to the sum of all the previous error currents. The sample and hold circuit shown in the upper part of the figure samples and stores this sum for addition at the end of the next cycle.

The nomenclature of Figure 3.2.3 will again be used in this analysis, where δV_1 is the error at the end of the first ramp period, δV_2 the error at the end of the second ramp period, and so on. One complete ramp period here shall be defined as the elapsed time between voltage peaks of the ramp. Recalling that I_0 is the charging current source and I_0' the discharging current source, the retrace time is

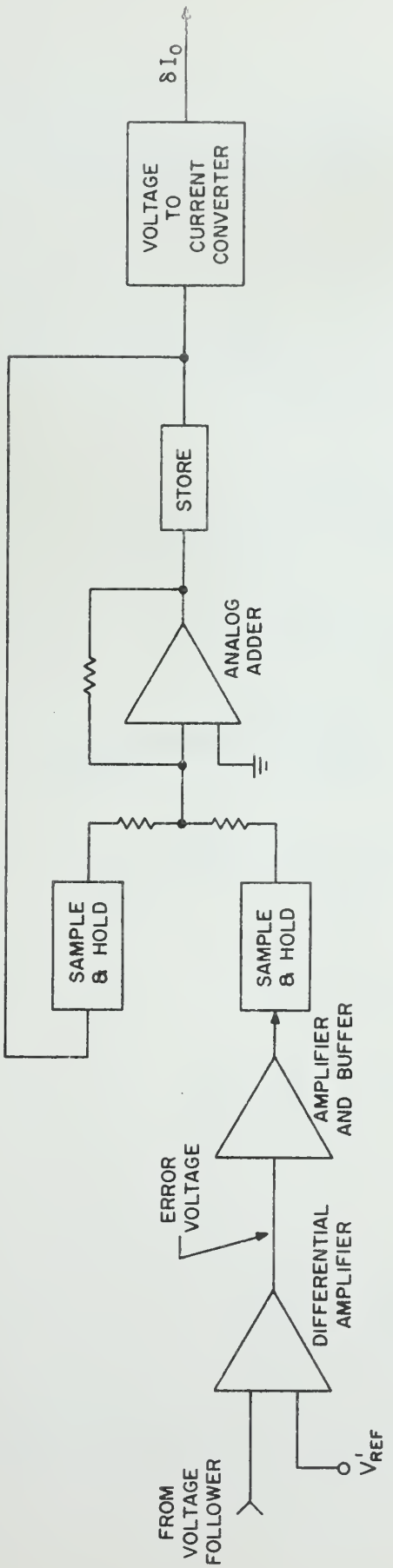


Figure A.4.1 Error Correcting Circuit

$$\frac{C(V - \delta V_{n-1})}{I_0' - I - (F\delta V_1 + F\delta V_2 + \ldots + F\delta V_{n-2})}$$

where $F\delta V_j$ is the error current generated during the jth cycle and held thereafter. F is the feedback factor expressed in amperes/volt. The duration of the positive going portion of the ramp is given by

$$\frac{C(V - \delta V_n)}{I + (F\delta V_1 + F\delta V_2 + \ldots + F\delta V_{n-1})}$$

The following relation is thus obtained:

$$T = \frac{C(V - \delta V_{n-1})}{I_0' - I_0 - (F\delta V_1 + F\delta V_2 + \ldots + F\delta V_{n-2})} + \frac{C(V - \delta V_n)}{I + (F\delta V_1 + F\delta V_2 + \ldots + F\delta V_{n-1})}$$

With no feedback applied it follows that

$$\frac{C(V - \delta V_1)}{I_0} + \frac{C(V - \delta V_1)}{I_0' - I_0} = T$$

which simplifies to

$$\frac{I_0 T}{VC} = \frac{1 - \frac{\delta V_1}{V}}{1 - \frac{I}{I_0'}}$$

Substituting this in the equation above and rearranging leads to the recursion relationship

$$\frac{\delta V_n}{V} = \frac{[I + \frac{FV}{I_0}(\frac{\delta V_1}{V} + \frac{\delta V_2}{V} + \ldots + \frac{\delta V_{n-1}}{V})](1 - \frac{\delta V_{n-1}}{V})}{\frac{I_0'}{I_0} - 1 - \frac{FV}{I_0}(\frac{\delta V_1}{V} + \frac{\delta V_2}{V} + \ldots + \frac{\delta V_{n-2}}{V})}$$

$$- \frac{1 - \frac{\delta V_1}{V}}{1 - \frac{I_0}{I_0'}}[1 + \frac{FV}{I_0}(\frac{\delta V_1}{V} + \frac{\delta V_2}{V} + \ldots + \frac{\delta V_{n-1}}{V})] + 1$$

Assuming some initial per cent error, this relationship may be employed to determine the amount of feedback required for the most rapid convergence to zero of the error voltage. The plots shown in Figure A.4.2 indicate that the most rapid convergence occurs for an initial feedback current $F\delta V_1$ which is ten per cent of the ramp charging current, assuming an initial voltage error of ten per cent.

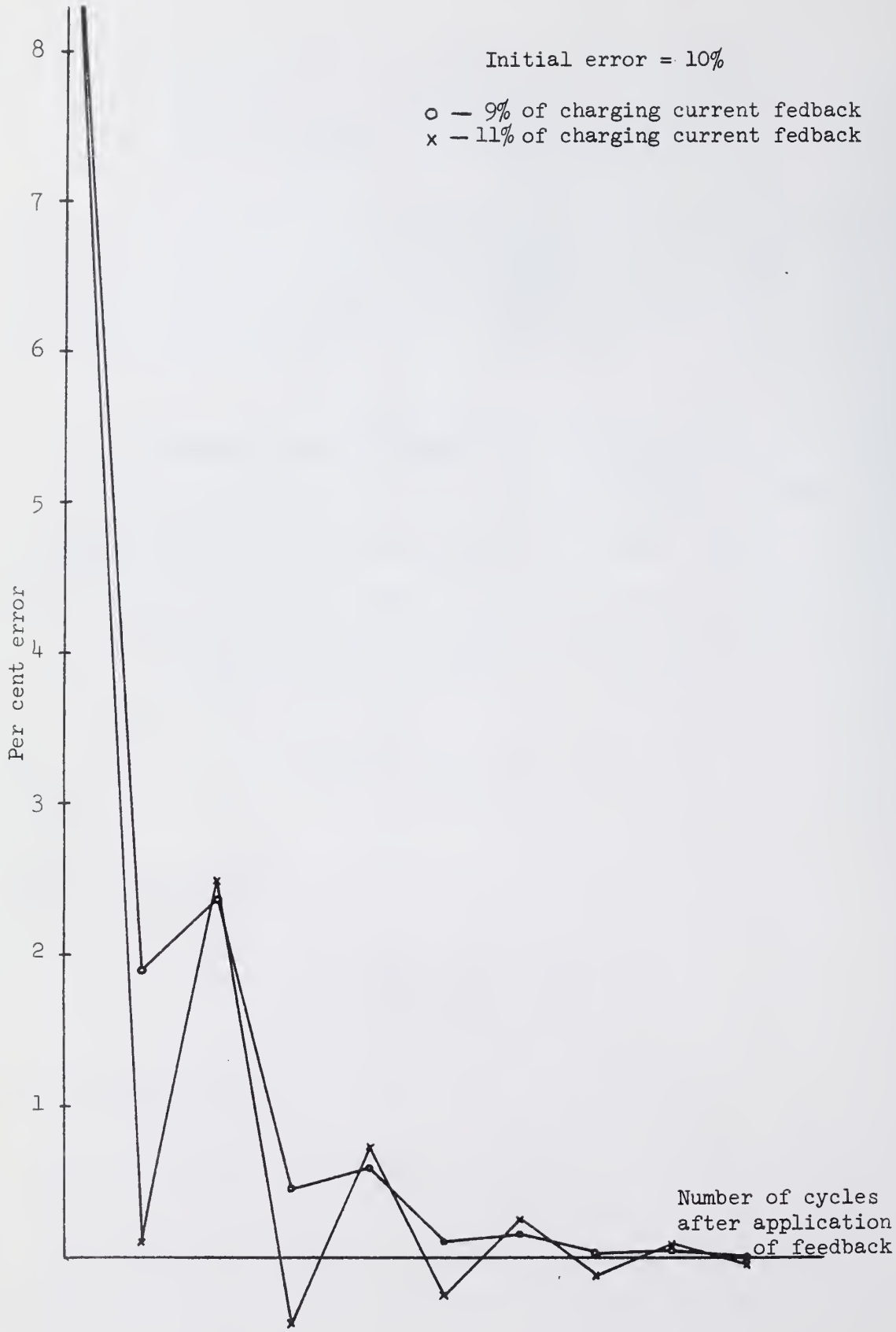


Figure A.4.2 Per cent Error Versus Number of Cycles Illustrating Convergence of Ramp Voltage Error

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